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RELIABILITY EVALUATION OF PROGRAMMABLE READ-ONLY MEMORIES (PROM--ETC(U)
SEP 77 K L WONG, W W POWELL, R L LONG F30602-75-C-0294
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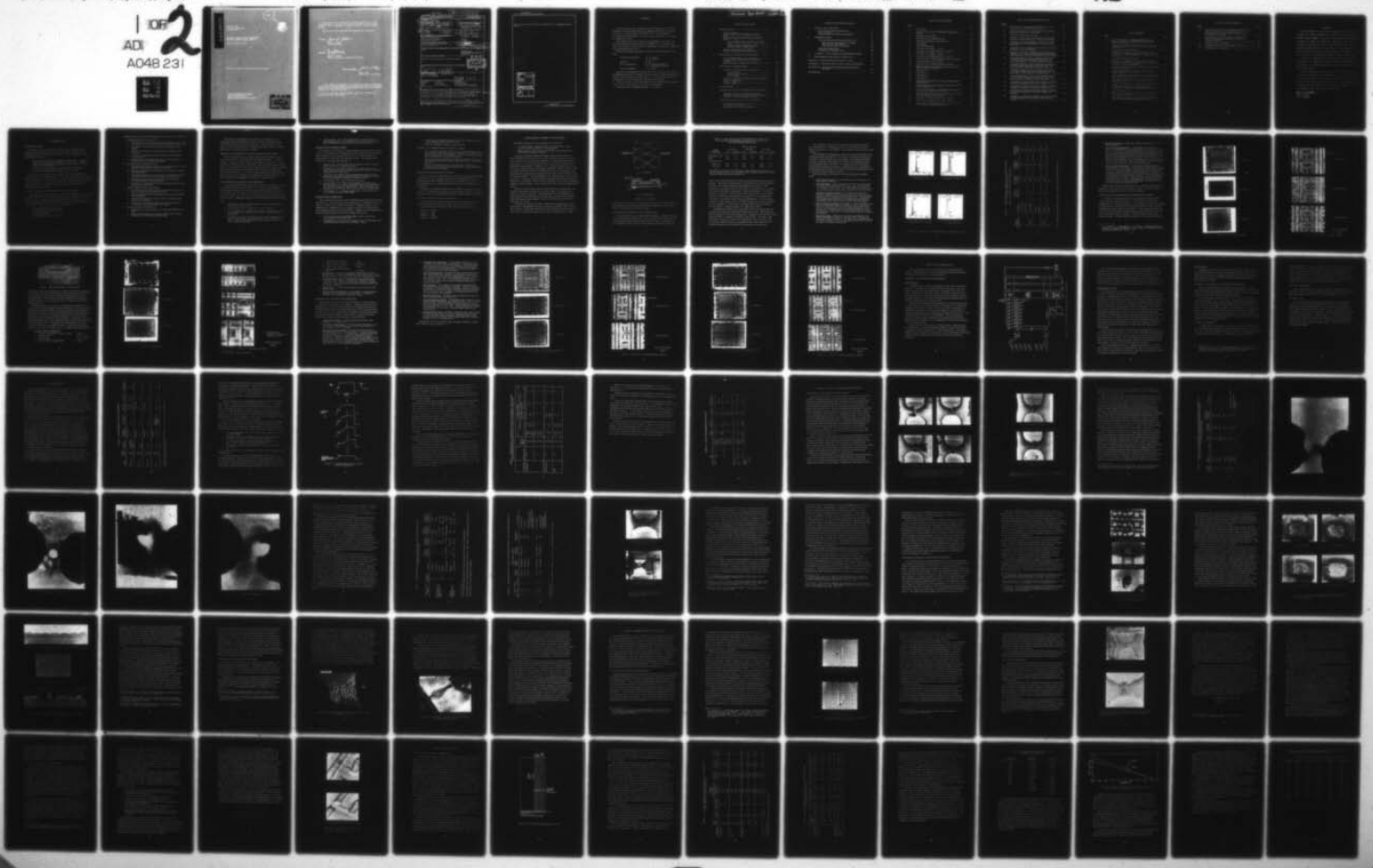

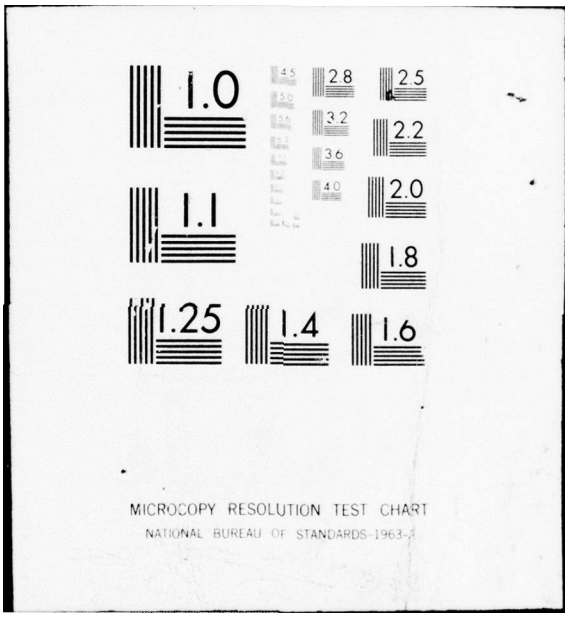
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RADC-TR-77-302
Final Technical Report
September 1977

RELIABILITY EVALUATION OF PROGRAMMABLE READ-ONLY MEMORIES (PROMs) PART II

Hughes Aircraft Company

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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Memory	Failure Rate	Polysilicon Fuse
PROM	Memory Programming	Avalanche-Induced-Migration
Screening Test		

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The primary objectives of this study were to: (1) Assess factors affecting the reliability of three types of Programmable Read-Only Memories (PROMs), namely Polysilicon Fuse, Avalanche-Induced-Migration (AIM) and Nichrome Fuse Technologies, (2) Investigate fusing and associated failure mechanisms and (3) Assess the reliability of these PROM's via a life test.

This study is a continuation of an earlier study on the reliability of PROM's which was completed in March 1975. The final report of the earlier study is

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RADC-TR-75-278, entitled, "Reliability Evaluation of Programmable Read-Only Memories."

PREFACE

This final report is the culmination of an 18 month study, Reliability Evaluation of Programmable Read-Only Memories (PROMs), commencing 17 June 1975 and terminating 17 December 1976. It is submitted in accordance with the provisions of Line Item A002, Exhibit A, for Contract No. F30602-75-C-0294.

The contents of the report represent the fulfillment of the above contract by the Strategic Systems Division of Hughes Aircraft Company and does not necessarily represent the recommendation, conclusions or approval of the United States Air Force.

The following Hughes personnel contributed to the completion of this work:

Principal Investigators:	W. W. Powell R. L. Long, Jr.
Advisor:	M. May
Project Engineers:	T. M. Donnelly (Phase I) P. C. McMahan (Phase II)
Program Manager:	K. L. Wong

Special acknowledgement is made to Dr. W. K. Jones for his assistance in obtaining thin sections of PROM chips and pictures of fuses through transmission electron microscopy, and to Mr. E. J. Fox for his recognition of the importance of this work and his continual encouragement.

Thanks also goes to all of the PROM users and vendors who contributed. Names of user-contributors are presented in the Appendix.

The RADC Project Engineer was Mr. J. J. Dobson.

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EVALUATION

The prime objective of this study was to establish effective reliability procedures for testing, qualifying and screening microcircuit programmable read-only memories (PROMs). This study evaluated programming fusing methods and materials to assess their reliability. PROMs using three types of programming (nichrome fusible link, avalanche-induced migrati (AIM) and polysilicon fusible link) were studied in detail. After programming the different devices with varying programming pulses and conditions, it was found that it was best to use manufacturer suggested voltages and waveforms.

The study is considered successful in meeting the initial objectives established at the beginning of the program. Personnel from Hughes that participated in this effort performed in a professional manner and produced a high quality report.

The major significance of this study is that it provides a background of technical understanding in the programming mechanism and failure modes of three types of PROMs. The findings of the study will be used in the preparation of MIL-M-38510 detail specifications for the PROMs studied in this program and for other PROMs which use the same type programming. The tests and programming methods will be added to MIL-STD-883.

James J. Dobson

JAMES J. DOBSON
Project Engineer

1. INTRODUCTION

PURPOSE OF STUDY

This final report presents the results of a study performed by the Strategic Systems Division of Hughes Aircraft Company under Rome Air Development Center Contract No. F30602-75-C-0294. The primary objectives of this study were:

1. Assess factors affecting the reliability of three types of programmable read-only memories (PROM's), namely polycrystalline silicon (polysilicon) fuse, avalanche-induced migration (AIM) and nichrome fuse technologies.
2. Investigate programming and associated failure mechanisms.
3. Assess the reliability of these PROM's via a life test.

This study is a continuation of an earlier study on the reliability of PROM's which was completed in March, 1975. The final report of the earlier study is RADC-TR-75-278, entitled, "Reliability Evaluation of Programmable Read-Only Memories." In that report three types of PROM's were covered, namely nichrome fuse, titanium-tungsten fuse and avalanche-induced migration (AIM) technologies.

SCOPE OF THIS PROM RELIABILITY EVALUATION STUDY

This study was conducted utilizing as vehicles ten 1024-bit, ten 2048-bit and five 4096-bit PROM's from each of four suppliers covering three technologies: Polysilicon fuse, avalanche-induced-migration (AIM) and nichrome fuse. Nichrome PROM's from two suppliers and the others from one supplier each were utilized. Four specific areas were investigated:

1. Programming and Electrical Test
2. Programming (Fusing) Mechanisms
3. Failure Mechanisms
4. Screening, Burn-in and Life Tests

Within these four areas, the following specific tasks were accomplished:

1. Programming and Electrical Test
   a. The unique electrical characteristics pertaining to programming were analyzed for each memory element technology under study.
   b. The effects of bit capacity/chip size on programming were studied.
   c. Methods of programming and their eventual reliability were evaluated.
   d. Concepts for optimizing programming yield and reliability were developed.
   e. Variations in programming pulses, such as fusing currents, and their effects on fusing were studied.
2. Programming (Fusing) Mechanisms
   a. Programming (fusing) mechanisms associated with each memory element technology under study were identified.
   b. Material and geometry characteristics of the memory elements were determined.
   c. Scanning electron microscope as well as transmission electron microscope studies of the fuse elements were performed.
   d. AIM devices were sectioned and junction shorting spikes after programming were photographed.
   e. Resistances of unprogrammed and programmed polysilicon fuse elements were measured.
3. Memory Element Failure Mechanisms
   a. Passivation integrity of fuse memory elements was studied by means of freeze-out and water drop tests.
   b. Reconduction likelihood of programmed fuse memory elements was investigated.
   c. Likelihood of unwanted shorting of memory element in AIM devices was evaluated.
   d. Likelihood of programmed AIM memory element opening or shorting of the isolation diode was studied.
4. Screening, burn-in and life tests
   a. Screening tests were performed on all fuse type PROMs under study.
   b. Burn-in and life tests were conducted under 125^{o}C chamber conditions for all PROM types under study.

The primary study emphasis was placed on the polysilicon fuse technology because this technology was not covered in the earlier study. The AIM technology received second priority. The nichrome fuse technology, which received the most coverage in the earlier study, was studied with respect to areas not already evaluated.

HISTORICAL BACKGROUND OF PROM TECHNOLOGIES STUDIED

The first field Programmable Read Only Memory (PROM) was introduced in early 1970. Today there are four different bipolar PROM technologies, at least 10 manufacturers, and more than 40 device types ranging from 256- to 8192-bit memory capacities. Basic variations in technologies relate to methods used to store a non-volatile memory bit. Memory elements may consists of nichrome fusible links, titanium-tungsten fusible links, polysilicon fusible links, or a reverse-biased emitter-base diode utilizing what is known as the Avalanche-Induced Migration (AIM) technology. The three technologies investigated in this study are discussed below.

Polycrystalline Silicon (Polysilicon) Fusible Links

The polysilicon film used to form the fuses in this technology is similar to that used in polysilicon gate MOS devices. Schottky bipolar PROMs utilizing this technology were introduced in the first quarter of 1972 and are now available from two vendors. The products of only one manufacturer, who offers military versions in 1024, 2048, and 4096-bit sizes, were tested in this program. Significant milestones in the development of this technology are:

1. First quarter 1974 - Circuit changes were made to increase the speed of the 1024-bit device.
2. Second quarter 1974 - 2048-bit device was introduced.
3. First quarter 1975 - Changed from diffusion of the base region to ion implantation for better process control. 4096-bit device was introduced.
4. Fourth quarter 1976 - 2048 and 4096-bit devices redesigned using polysilicon crossunders to enable smaller chip sizes and higher speed. (Devices were obtained for this program in 1975 and did not have this modification.)

5. Fourth quarter, 1976 - The manufacturer's recommended programming algorithm was modified to increase programming yield. (This modification was not used in the tests reported here.)

Avalanche-Induced Migration (AIM)

The AIM memory element is a diffused bipolar transistor without a base contact. Programming is accomplished by electrically altering the emitter-base junction to form a resistive short across it. This technology was introduced in 1971 with 1024 and 2048-bit versions. The principal milestones in its subsequent development are:

1. January 1972 - The 1024-bit chip was reduced in size to improve speed and increase programming yield.
2. February 1973 - Circuitry changes were made to improve chip enable speed and reduce programming path resistance and required voltage on the 1024-bit device.
3. June 1974 - The number of after programming pulses which are applied after the emitter-base short has been sensed was reduced to prevent degradation of the base-collector junction.
4. First quarter 1975 - 4096-bit device introduced.
5. Second quarter 1976 - Minor mask changes were made on the 4096-bit device to increase its speed and improve the high temperature operation of the chip enable driver. (Devices tested in this program were obtained in 1975 and did not have this modification.)
6. 1 November 1976 - A military specification, MIL-M-38510/202, was issued for 1024-bit AIM PROMs.

Nichrome (NiCr) Fusible Links

This technology is the first used for PROM elements and was introduced in April 1970. It is now in use by six manufacturers, although products from only two of them were included in this study. Complete accounts of each manufacturer's design and process changes are difficult to obtain because of the proprietary nature of the information. Changes in NiCr PROM design and processing reported in the previous Hughes study were:

1. Use of a new process to provide tighter control of the cross-sectional area of the fusible link.
2. Implementation of a new screen utilizing a bias to test fusible links contained in each device (not accessible to users).

3. Verification of programmed patterns utilizing a reduction in power supply voltage (to approximately 4 volts).

4. Utilization of double masking to reduce pinholes.

Recently, three additional developments have occurred:

5. The 1024, 2048, and 4096-bit devices of both manufacturers have been revised so that they form generic families, i.e., they all use similar layouts and circuit designs. Various circuit improvements were incorporated in the generic designs.

6. Improvements in programming circuits and manufacturing test procedures have been made to enable single pulse progr ming with high yield.

7. Both NiCr PROM product lines included in this study now use Schottky diode clamps instead of gold doping to achieve high speed and/or low power operation.

MILITARY SPECIFICATIONS FOR PROMS

The U.S. Air Force specification for 512-bit nichrome fuse link PROMs is MIL-M-38510/201, issued 21 August 1972 and amended 17 July 1973. The specification MIL-M-38510/202, issued 1 November 1976, is for 1024-bit AIM devices. Additional USAF specifications for PROMs are in preparation.

Department of Defense specifications for PROMs were issued 30 January 1976. The general specification is drawing number ON126296. Detail requirements for 1024-bit PROMs are given in drawing number ON126296/01.

VENDORS OF DEVICES USED IN THIS STUDY

The four vendors of devices used in this study are Harris Semiconductor; Monolithic Memories, Inc.; Intel Corp.; and Intersil, Inc.

The following codes are used in this report for vendor designation:

Vendor A = Harris

Vendor B = MMI

Vendor X = Intel

Vendor Y = Intersil

2. PROM MEMORY ELEMENT TECHNOLOGIES

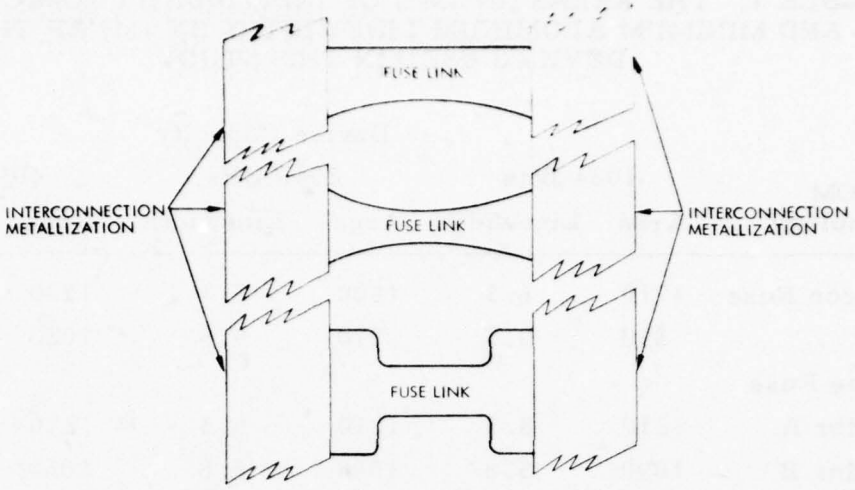
The PROM element structures included in this study are

1. Fuse Link PROMs, employing either nichrome (NiCr) or polycrystalline silicon (polysilicon) fuse materials.
2. AIM (avalanche-induced migration) PROMs, often referred to as "blown diode" memory elements.

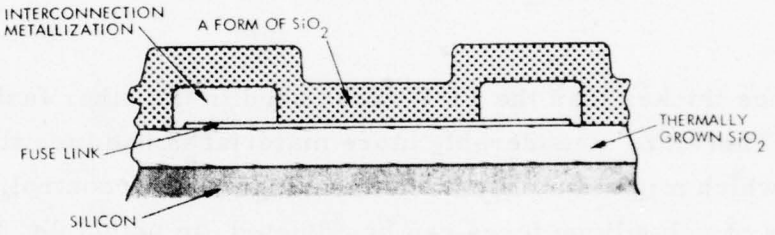
A survey of available fusible link PROMs indicates that a variety of different shaped fuse links are used. In part, the differences occur because of fuse material selection and/or composition. Programming reliability is also a factor. Fuse link material thickness, cross-section, length between opposed termination pads, resistance, etc., all may affect fuse link ease of fabrication, programmability and ultimate reliability. Material selection and associated fabrication processes do affect the occurrence and frequency of potential failure modes such as unprogrammed "opens" and "growback" links or unwanted "shorts." An understanding of fuse configurations, materials and processes is, therefore, quite necessary in generating an accurate picture of PROM device reliability. Top views and a sectional view of a fuse link along its length are shown in Figure 1; the vertical scale of the section is exaggerated for clarity.

The AIM or blown emitter-base junction PROM is quite different in concept and configuration from the fuse link type PROM. The AIM memory element is a planar transistor. Programming is effected by high current pulses which permanently short the emitter-base junction of the transistor. Thus the programming mechanism occurs below the surface of the device, within the bulk silicon.

Following are details of the three PROM element technologies included in this study. Photographs of the devices used are included. The areas of the cells which contain the individual memory elements are listed in Table 1. The memory arrays also contain some Al buses, typically one per eight



a. Top views



b. Sectional view

Figure 1. Fuse links.

columns of cells, which are not included in the cell areas. The widths of the aluminum lines (which are the electrical connections to each column of cells in the array) are also given in Table 1.

POLYCRYSTALLINE SILICON FUSE TECHNOLOGY

The polysilicon fuses are shaped like an hourglass, similar to the fuse shown at the bottom of Figure 1a. Their minimum width is about half the width of the NiCr fuses and the same as for Ti-W fuses. However, the polycrystalline Si film is about 16 times thicker than the NiCr films and

TABLE 1. THE AREAS (IN μM^2) OF INDIVIDUAL PROM CELLS AND MINIMUM ALUMINUM LINEWIDTHS (IN μM) OF THE DEVICES USED IN THIS STUDY

PROM Technology	Device Capacity 1024 Bits Area	1024 Bits Linewidth	2048 Bits Area	2048 Bits Linewidth	4096 Bits Area	4096 Bits Linewidth
Polysilicon Fuse	1710	6.3	1500	5.3	1500	6.3
AIM	850	9.5	970	9.5	1020	12.7
Nichrome Fuse						
Vendor A	1210	5.3	1210	5.3	1270*	4.8*
Vendor B	1090	5.8	1090	5.8	1060*	5.0*

*The differences between the dimensions of the nichrome 4096-bit devices and the smaller devices from the same vendor probably result from normal manufacturing and measuring tolerances.

about 4 times thicker than the Ti-W films used in the other fusible link technologies. Therefore considerably more material is used for the polysilicon fuse link, which might simplify manufacturing process control. The resistances of polysilicon fuses can be adjusted, in principle, by controlling the amount of phosphorus doping that is subsequently applied. In practice, however, the polysilicon film is doped at the same time as are the emitters of the n-p-n transistors and therefore its resistivity is not independently controlled. The polysilicon film extends underneath the Al column address conductors on the memory array. (On devices made since the fourth quarter of 1976, polysilicon is used to form crossings under Al lines on 2048 and 4096-bit devices, enabling smaller size, higher yield chips.)

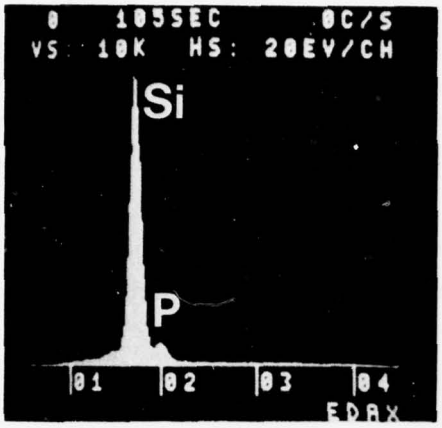
A phosphosilicate glass film is deposited on top of the metallization for protection from abrasion and particles inside the package. When this glass film is etched away at the chip bonding pads, openings are also etched at every polysilicon fuse, reportedly to facilitate programming. The native oxide that forms on silicon will protect the exposed fuses from corrosion. The even thicker oxide that forms on programmed fuses while they are hot is probably sufficient to protect them from shorting by loose particles.

The composition of the various components of the memory elements was investigated by a scanning electron microscope (SEM) using energy dispersive analysis of x-rays (EDAX). The resulting x-ray spectra are shown in Figure 2.

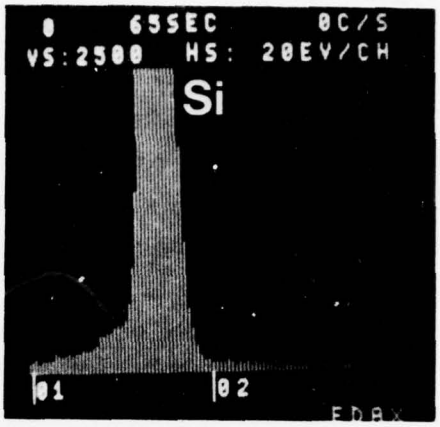
The resistances of unprogrammed fuses were measured with two needle probes and a Tektronix Type 576 Curve Tracer. The data are summarized in Table 2. The resistances of the unetched (as-received)samples ranged from 70 to 122 ohms with an average of 89 ohms, in reasonable agreement with the nominal value of 100 ohms. The reason for the etched resistors being of lower resistance is not known; perhaps it is due to contamination of the polysilicon by the etchant or formation of a parallel conductive path on the bare (except for native oxide) Si substrate.

The characteristics of the polysilicon fuse technology are detailed below:

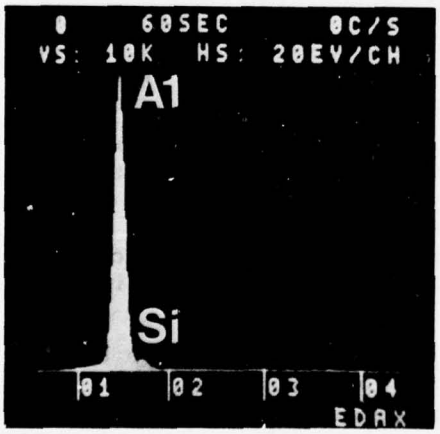
1. Field Oxide Thickness - The thermally-grown Si wafer oxide coating is about 0.3 μm thick.
2. Fuse Dimensions - The average width of the neck of the fuse links is 2.2 μm, with a standard deviation of ±0.5 μm. The probability of having links narrower than 1 μm, which might be fused by the read current, in only 0.01 percent. The length of the link is about 7 μm and the thickness of the polysilicon film is 0.35 μm ± 0.04 μm.
3. Polysilicon Deposition Method - Vapor phase chemical vapor deposition, similar to that used for polysilicon gate MOS devices, is used to deposit the polycrystalline silicon film. No intermediate adhesion layer is used underneath the polysilicon. The fuses are subsequently doped with phosphorus during the emitter diffusion step, which gives a sheet resistance of 50 to 100 ohm/square.
4. Fuse Terminations and Interconnections - A film of aluminum, 1 μm thick, is used to form the fuse terminations and circuit interconnections. Polysilicon underlies only the Al column buses on the array. The Al-polysilicon interface is approximately 8 x 14 μm. The interface is located at the termination pad on the end of each transistor fuse. Low contact resistance at this interface is obtained by sintering.
5. Passivation Glass - Phosphosilicate glass, approximately 1 μm thick, is deposited by chemical vapor deposition. The nominal phosphorus content is 2 percent. The glass is subsequently removed by chemical etching from the bonding pads and from every fuse link (in order to facilitate programming).



a. Passivation glass



b. Oxide on silicon



c. Aluminum interconnection

d. Polysilicon fuse

Figure 2. Polysilicon fuse PROM: SEM-EDAX composition results.

TABLE 2. RESISTANCES OF UNBLOWN POLYSILICON FUSES
1024-BIT PROM DEVICES

(Contact resistances have been subtracted)

Sample Designation	Condition	Number of Fuses Measured	Average Resistance (ohm)	Minimum Resistance (ohm)	Maximum Resistance (ohm)
1	As received	8	80 ±8	70	94
2	As received	6	100 ±14	84	122
1 and 2	As received	14	89 ±14	70	122
3	Etched*	6	57 ±9	50	74
4	Etched*	8	70 ±6	60	79
3 and 4	Etched*	14	64 ±10	50	79
D	Etched*	1	40	–	–

*For 1 minute in buffered HF to remove overglass and oxide for SEM analysis.

6. PROM Die Separation - Diamond scribing and breaking are used to dice the wafers.

7. Fuse Programming and Test - The nominal fusing current[1] is 30 mA, corresponding to a current density of 4×10^6 A/cm^2 at the neck of the fuse link. The programming power is normally about 90 mW. The temperature at the center of the polysilicon fuse during programming has been calculated to be above the melting point of silicon[1] and good agreement between observed and calculated fusing times has been obtained. An extra row and column of fuses are provided at the perimeter of each PROM array for test programming, which is done at the wafer stage, before dicing. Functional testing is also performed before dicing and after packaging.

8. Memory Element Properties - The nominal unprogrammed fuse link resistance is 100 ohms. Variations in the sheet resistance of the polysilicon and the dimensions of the fuse result in actual values of 50 to 150 ohms (cf. Table 2). Programmed fuses usually have resistances greater than 10^9 ohms (cf. section 5). The read-out (sensing) current is nominally 2 mA[1] and the voltage available at the fuse is about 2V, so the minimum resistance for a fuse to appear programmed is 1000 ohms. The actual read-out current sensitivity may be as low as 0.5 mA, corresponding to a fuse resistance of 4000 ohms, which is therefore the maximum resistance at which a fuse may appear to be unprogrammed.

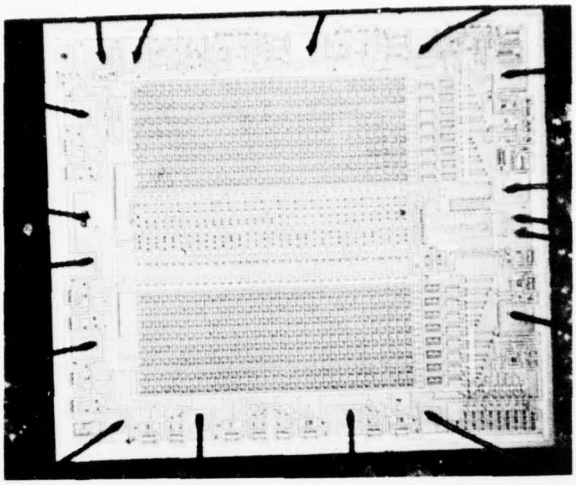
Photographs of the three different size chips and the individual memory elements on each chip are shown in Figures 3 and 4. Note the openings in the passivation glass at every fuse location in Figure 4.

AVALANCHE-INDUCED MIGRATION (AIM) MEMORY ELEMENT

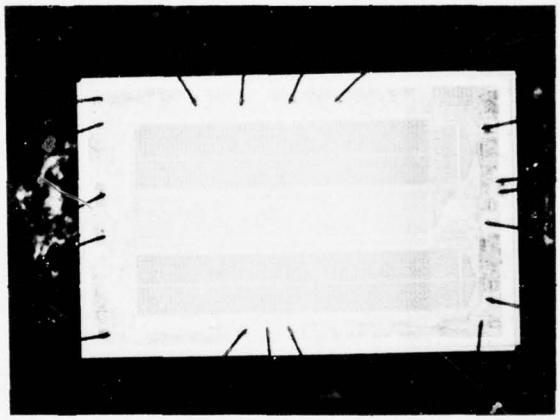
A schematic sectional view of the n-p-n transistor used as the AIM memory element is shown in Figure 5. (The vertical scale has been exaggerated for clarity in this drawing.) Programming is effected by passing a relatively large current (200 mA) through the transistor with the emitter voltage positive with respect to the collector. This current passing in the reverse direction through the emitter-base junction results in a permanent short across that junction, leaving a p-n (base-collector) diode at that memory location. A small sensing current (0.5 mA) is passed through the

---

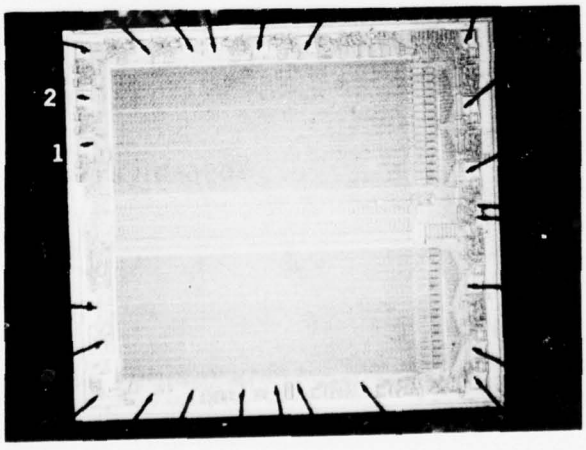
1. R. C. Smith, S. J. Rosenberg, C. R. Barrett, "Reliability Studies of Polysilicon Fusible Link PROM's," Proc. IEEE 1976 Reliability Physics Symposium (IEEE, NY, 1976), p. 193.



a. 1024 bits

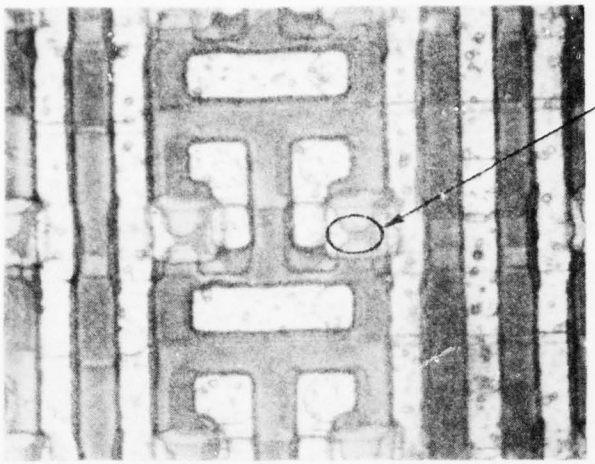


b. 2048 bits

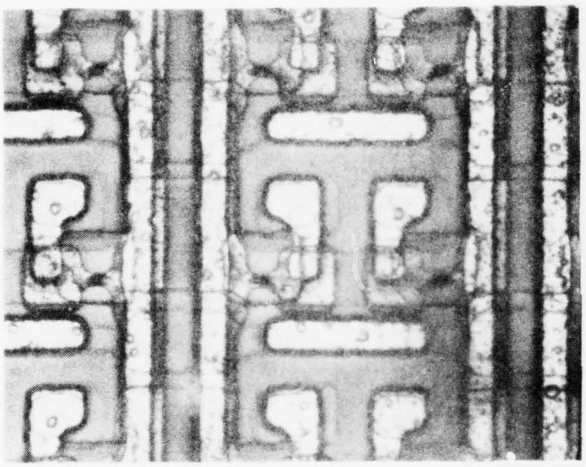


c. 4096 bits

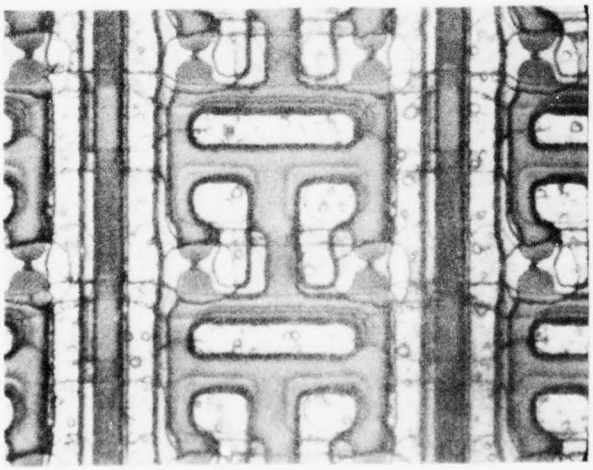
Figure 3. Polysilicon fuse PROM.



a. 1024-bit device



b. 2048-bit device



c. 4096-bit device

Scale for this page:

25μm

Figure 4. Polysilicon fuse PROM elements.

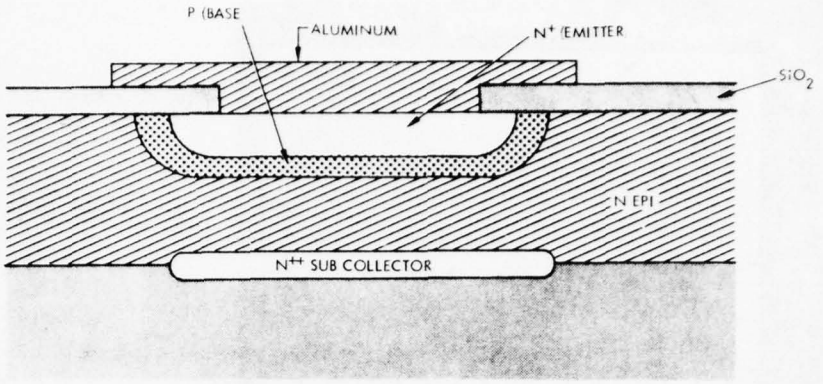


Figure 5. AIM memory element, sectional view.

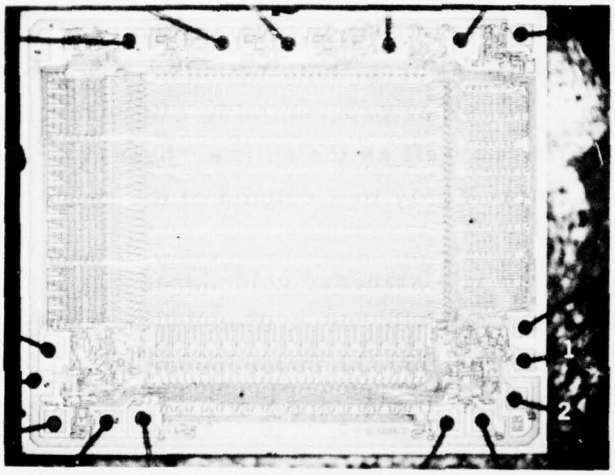
element after each programming pulse in order to detect when programming is completed, after which four additional programming pulses are passed to insure permanent programming. Improper programming can result in shorting the base-collector junction as well as the emitter-base junction, thereby shorting a row of the memory array to a column of the array and disabling the device.

The manufacturing process used is a standard gold-doped bipolar TTL device process without the additional thin film deposition and patterning steps required for fusible link PROMs. (Note that the latter devices included in this study use Schottky diodes rather than gold doping to obtain high speed transistors.) Two levels of aluminum metallization are used in order to utilize the inherent high density of this technology. A phosphosilicate glass film is used between the two Al metallization layers and as a passivation layer on top of the upper layer. Photographs of the three different size chips included in this study are presented in Figure 6. Individual programming elements on each chip are shown in Figure 7. Details of this technology are:

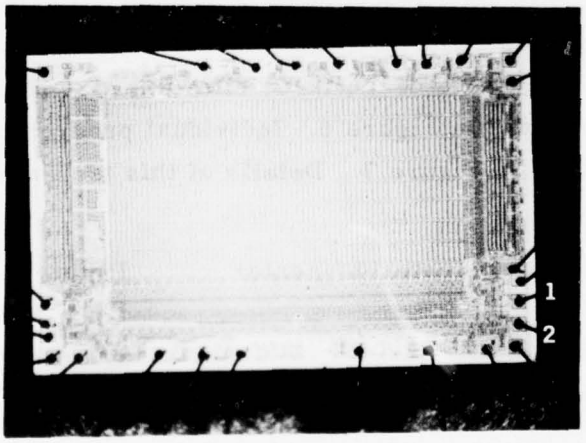
1. Memory element configuration

a.	Spacing of transistors, center-to-center	18 μm
b.	Emitter depth	1.5 - 1.9 μm
c.	Base thickness	0.3 - 1.0 μm
d.	Buried collector channel width	18 μm

a. 1024 bits

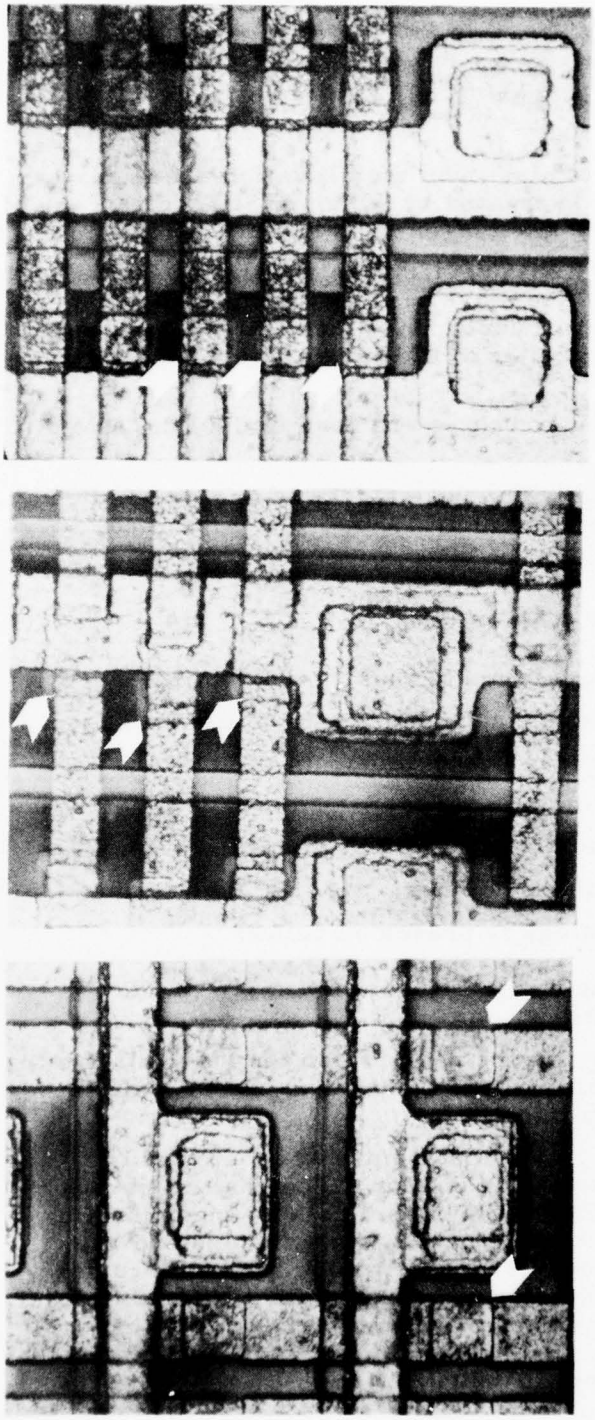


b. 2048 bits



c. 4096 bits

Figure 6. AIM PROM.



a. 1024-bit device

b. 2048-bit device

c. 4096-bit device
(Rotated 90 degrees with respect to a and b)

Scale for this page:

25μm

Figure 7. AIM PROM elements.*

*Some emitter contacts indicated.

e.	Epitaxial layer thickness	6 μm
f.	Size of collector contacts	12 x 25 μm
g.	Width of Al conductors	9 μm
h.	Base-emitter junction area (approx.)	5 x 5 μm

2. Metallization - Two levels of aluminum metallization are used, each 1 μm thick. They are separated by 70 nm of SiO_2, plus 1 μm of phosphorus-doped SiO_2, deposited by chemical vapor deposition (CVD).
3. Passivation Glass - Military AIM devices are passivated with a 1 μm thick CVD overglass. This layer is a sandwich structure, consisting of SiO_2, phosphorus-doped SiO_2, and SiO_2. Sintering of the Al-Si contacts for 4 minutes at 425°C is performed after the passivation is deposited.
4. Die Separation - Scribing and breaking are used to dice the AIM PROM wafers.
5. Memory Element Resistance - The resistances of unprogrammed elements are in the neighborhood of 10^9 ohms. Programmed junctions have a resistance of less than 10 ohms.

NICHROME (NiCr) FUSIBLE LINK TECHNOLOGY

Nichrome fuse links are made in various shapes, as shown in Figure 1, according to each manufacturer's preference. Variations in the thickness and Ni:Cr ratio of the nichrome film may occur among manufacturers and for different date codes of the same manufacturer. Due to the long interest in electro-corrosion of nichrome films, the quality of the passivation glass has received particular attention in these devices. Specific information about this very popular PROM technology is presented below:

1. Field Oxide Thickness - The thermally-grown Si wafer oxide coating is 0.6 - 0.8 μm thick.
2. Nichrome Fuse Dimensions - In the neck region the fuse is 3.1 to 5.1 μm wide. The fuse itself is 10 to 25 μm long and the NiCr fuse material is 15 to 25 nm thick.
3. Nichrome Deposition Method - No metal interface material is required beneath NiCr to improve adhesion. Thermal evaporation is used to deposit NiCr on the PROM wafer, followed by annealing at elevated temperature. Actual annealing temperature and duration are considered proprietary information by suppliers, as this process is used to provide a homogeneous distribution of nickel and chromium within the fuse material film, thereby reducing programming problems. Suppliers use crystal oscillator film thickness monitors for controlling NiCr depositions.

4. Nichrome Film Composition - Spectrographic analysis is used to verify the composition of the nichrome films. One supplier using nichrome fuses states that the most stable fuses which provide the most repeatable programming results are those made of approximately 50 percent Ni and 50 percent Cr. The exact composition is considered proprietary by the suppliers.

5. Fuse Termination Pads - Aluminum is used as the termination pad and conductor material contacting each end of the nichrome fuse link. Termination pad thickness is approximately 1 μm. The area of conductors making contact with fuse termination pad ends is approximately 5 μm x 6 μm. No information is available on the contact resistance between the aluminum termination pads and the nichrome fuse links.

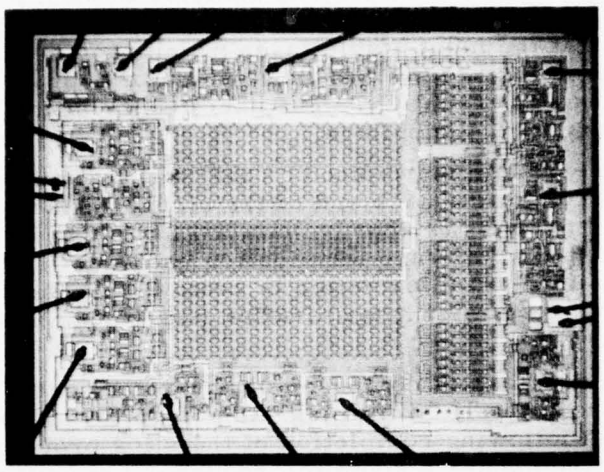
6. Fuse Overglass - The overglass is composed of phosphosilicate glass (silox) and is approximately 1 μm thick. The fuse overglass is inspected for pinholes following completion of the silox processing. PROM wafers are examined under a zoom microscope at magnifications of more than 100x. In general, no additional tests are used to ensure overglass film integrity.

7. PROM Die Separation - Diamond, laser and single-wheel saws are used to separate wafers into PROM dice.

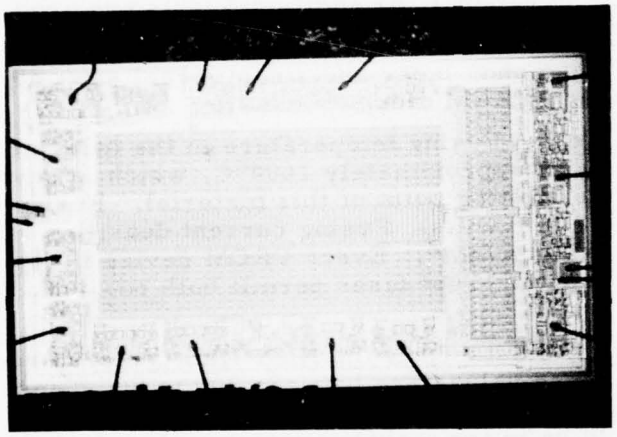
8. Fuse Programming and Test - Fusing temperature in the fuse "neck" region has been calculated at approximately 1600°C, which is several hundred degrees above the melting point of this material. Fusing voltage is approximately 7 to 8 volts. Fusing current densities have been estimated at $2 - 5 \times 10^7$ A/cm^2. Every PROM device is tested at both the wafer and die level. Test fuses permit both row and column checks.

9. Fuse Resistance Values - Resistance of the NiCr film centers around 100 ohms/square; actual fuse values are between 300 to 500 ohms including photolithographic variations. When programmed open, the fuse resistance should be in the megohm region with a workable minimum down to around 4000 ohms.

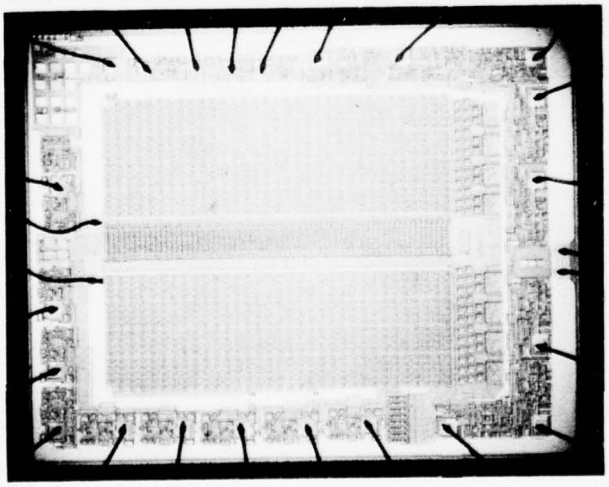
Photographs of the nichrome fuse chips and memory elements included in this study are given in Figures 8 - 11.



a. 1024 bits

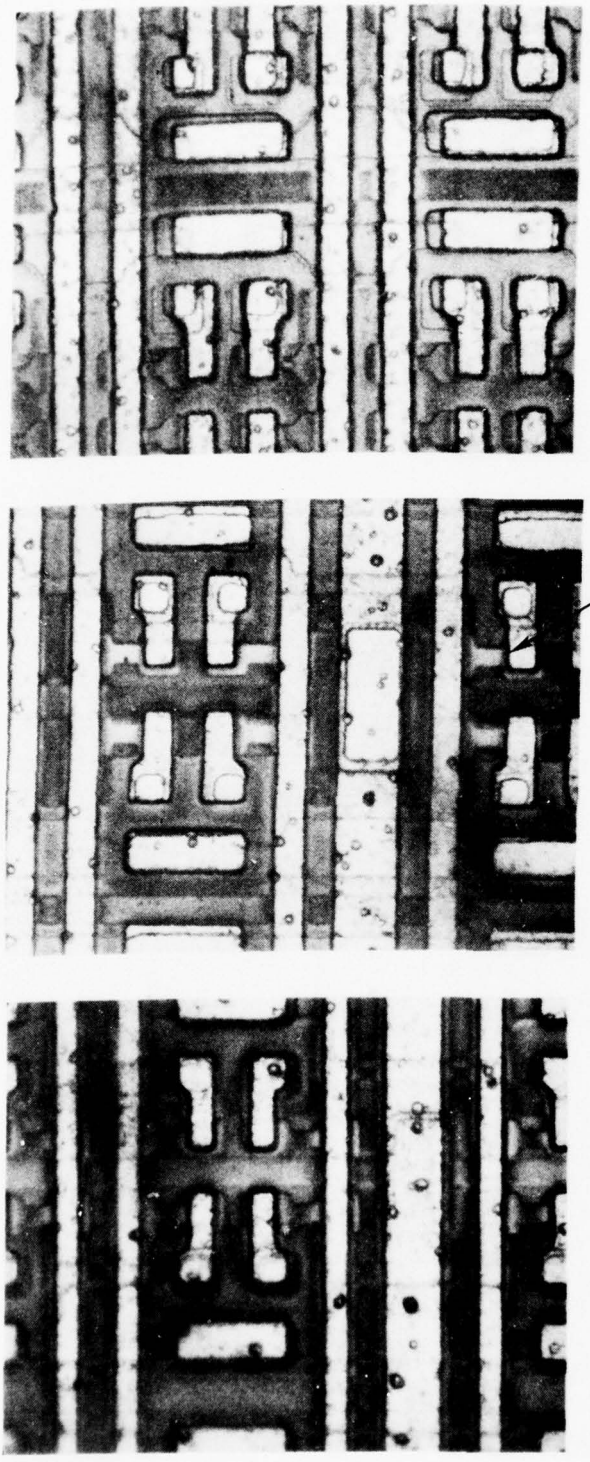


b. 2048 bits



c. 4096 bits

Figure 8. Nichrome fuse PROM, vendor A.
(See page 5 for vendor codes.)



a. 1024-bit device

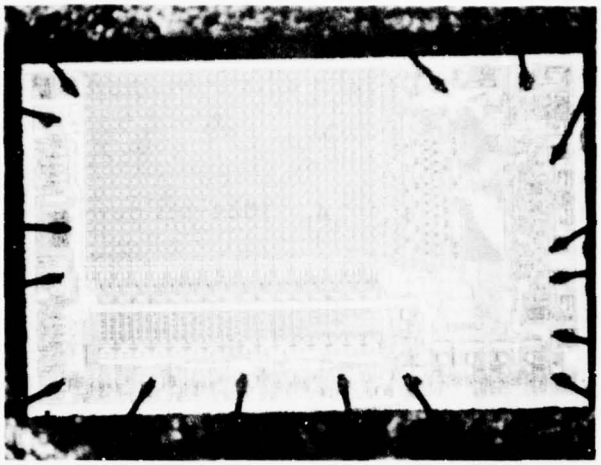
b. 2048-bit device

c. 4096-bit device

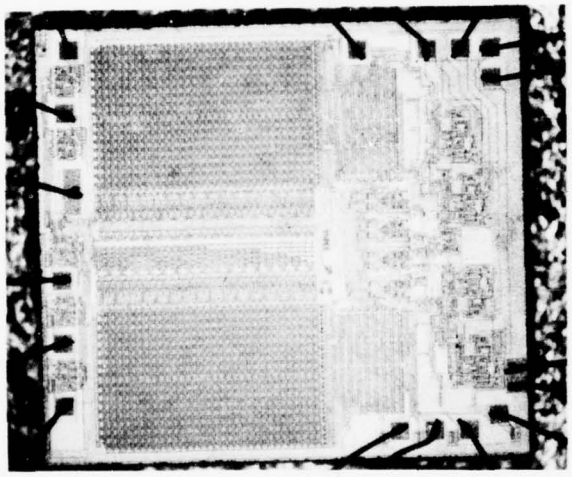
Scale for this page:

25μm

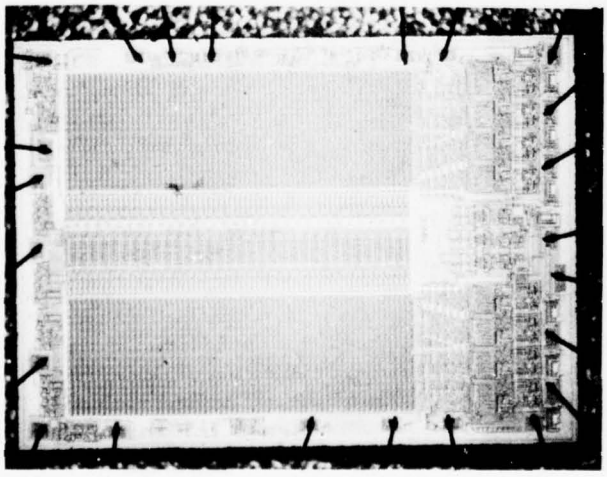
Figure 9. Nichrome fuse PROM elements, Vendor A.



a. 1024 bits

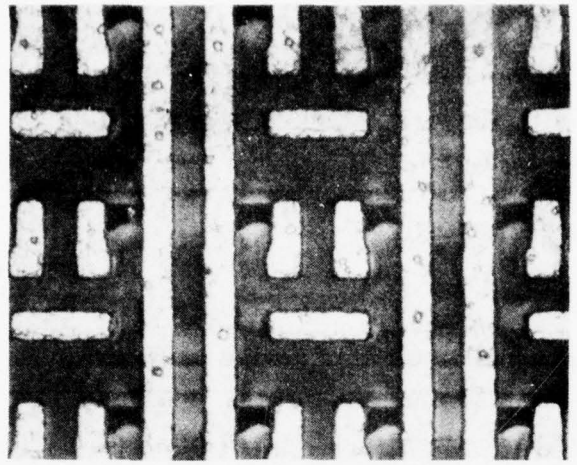


b. 2048 bits

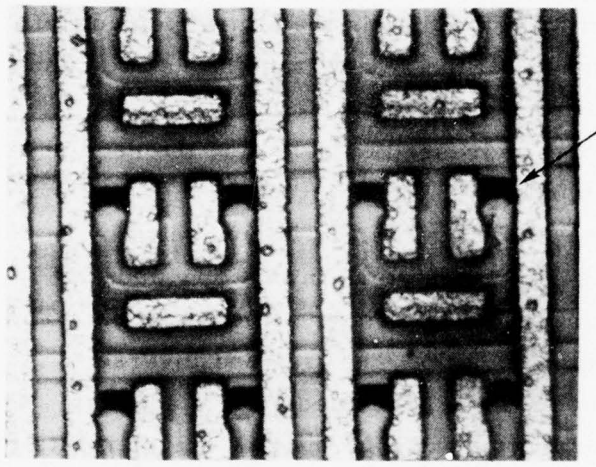


c. 4096 bits

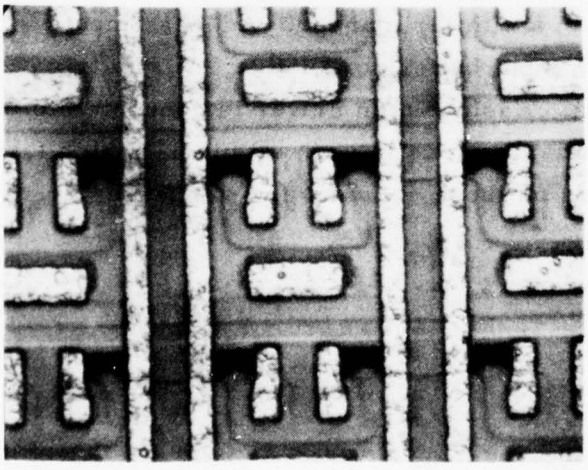
Figure 10. Nichrome fuse PROM, vendor B.
(See page 5 for vendor codes.)



a. 1024-bit device



b. 2048-bit device



c. 4096-bit device

Scale for this page:

25μm

Figure 11. Nichrome fuse PROM elements, vendor B.

3. PROM CIRCUIT DESCRIPTIONS

The circuit design and layout of the devices are described in this section. This information is useful in the understanding of programming difficulties and performance of failure analyses.

VENDOR X - 1024-BIT DEVICE (POLYSILICON)

Read Circuitry

A skeletal outline of the circuit schematic for this device is shown in Figure 12. The memory is organized as 256 four-bit words. The fuse matrix is partitioned into four blocks that correspond to the 4 bits; each block contains 32 rows and eight columns. The address selection scheme uses one transistor per fuse location with the fuse in the emitter circuit of the select transistor. The collectors of all the select transistors are connected in common to the V_{cc} voltage source.

The desired 4-bit memory word is addressed by selecting the required row and column in each of the four blocks. The proper row is selected by turning on one of the 32 row drivers. Each row driver is connected by a common bus to the bases of all the select transistors in that row and, if selected, provides base drive to eight select transistors in each block. The row drivers have the character of an AND gate. The true and inverse functions of address inputs A_3 through A_7 are generated by five address buffers and are connected in various combinations to the row driver inputs to form a row select matrix.

Column selection is performed in a similar manner. Address inputs A_0 through A_2 are connected through input buffers to another AND matrix to select one of eight column drivers. Each column driver is connected to the bases of four column select transistors, one in each bit block, which form a series connection between the fuses on those columns and the sense amplifiers.

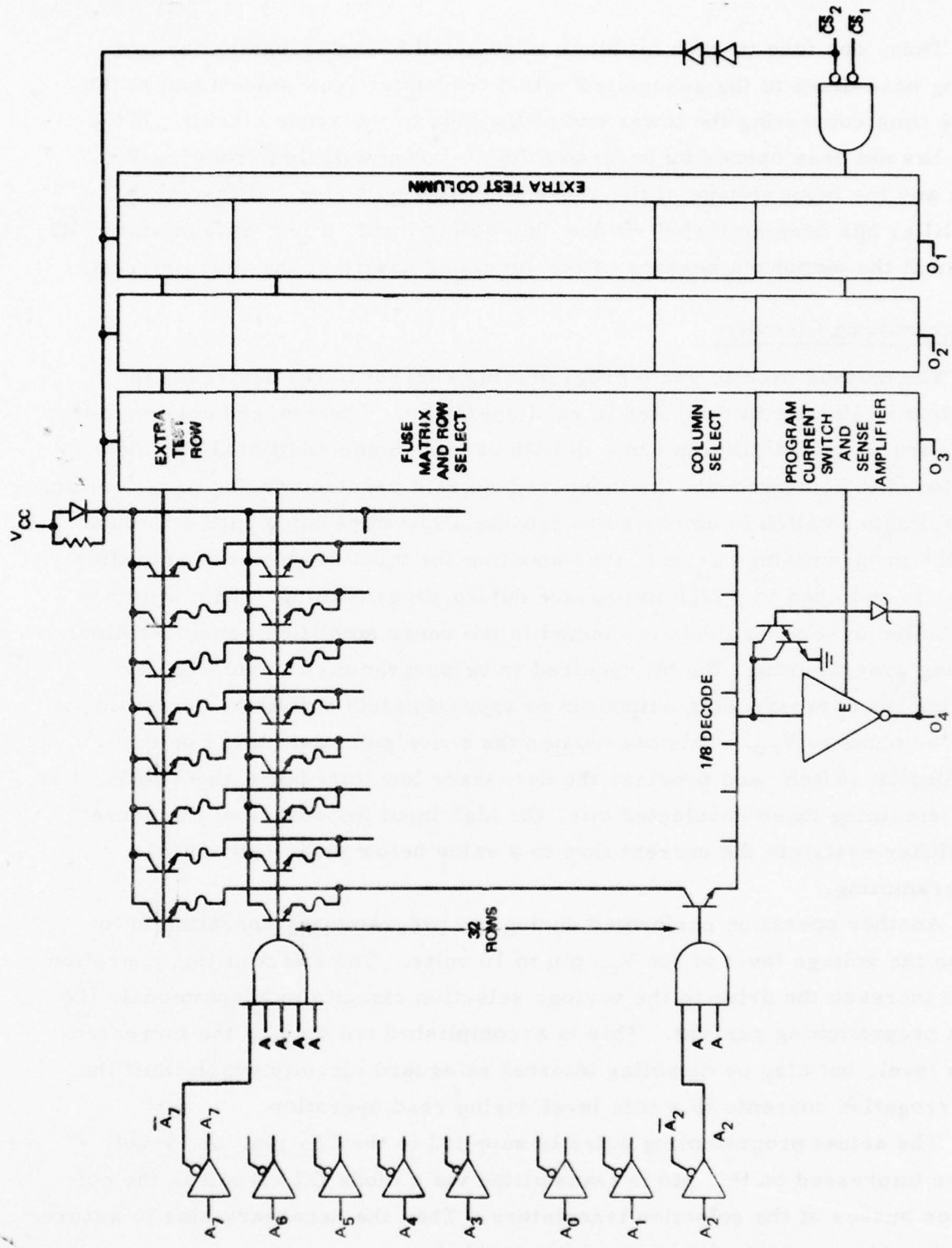


Figure 12. Vendor X 1024-bit PROM skeletal circuit schematic.

Thus, one fuse in each bit block is selected for interrogation by providing base drive to the associated select transistor (row select) and at the same time connecting the lower end of the fuse to the sense circuit. If the fuse has not been opened by programming, current will flow from the V_{cc} node and the input voltage of the sense amplifier will rise. If the sense amplifier has been activated via the chip select input, a low voltage state will occur at the output pin because of the inverting nature of the sense circuit.

Programming Circuitry

The method used to route programming current to the desired fuse location is similar to that used in read operation. The row and column select circuitry is essentially the same in both cases. Some additional circuitry is employed to accommodate the increased current required during programming. A Darlington switch is employed to provide a low impedance path to ground for the programming current, thus shunting the input of the sense amplifier which is switched to a high impedance during programming. This switch is controlled by a zener diode connected to the sense amplifier output terminal. During programming, the bit required to be programmed is selected by raising the corresponding output pin to approximately 8 volts by connecting it via 300 ohms to V_{cc}. This overcomes the zener potential, turns on the Darlington switch, and provides the necessary low impedance shunt path. For the remaining three unselected bits, the high input impedance of the sense amplifier restricts the current flow to a value below that required for programming.

Another operation performed during the programming operation is to raise the voltage level of the V_{cc} pin to 10 volts. The effect of this operation is to increase the drive to the various selection circuits to accommodate the high programming current. This is accomplished not only by the increased bias level, but also by disabling internal safeguard circuits which limit the interrogation currents to a safe level during read operation.

The actual programming pulse is supplied to the CS_2 pin. A 15-volt pulse impressed on this pin is transmitted via a diode OR circuit to the collector busses of the selection transistors. Then the necessary bias to assure an adequate programming current is provided.

Test Circuitry

Examination of the chip reveals that an extra row and column of fuses and associated selection circuits are provided on the chip. These were included by the vendor as a quality control feature so that the programming characteristics of the chip could be measured without destroying fuses in the main memory matrix.

VENDOR X – 2048 AND 4096-BIT DEVICES (POLYSILICON)

The general design approach for these devices is the same as that described for the 1024-bit device in the previous paragraphs. The principal differences are in the organization for greater capacity, a few circuit design changes, and the addition of a power switching feature.

The sense amplifier in these devices is non-inverting, so that a programmed bit results in a low level output. An additional voltage clamping circuit on the column busses has been added which operates during the read mode. The 2048-bit device is organized into 512 words of 4 bits each, so that 64 row select drivers are required. The 4096 bit device is organized as 512 x 8, so that 8 bit blocks (64 x 8) were required. The power switching feature added to both of these devices (available as an option) consists of a switch controlled by the chip select inputs which reduces the required power supply current in the deselected mode.

VENDOR B (NICHROME)

An outline of the circuit design of the 1024-bit version of these devices was presented in the Final Report of an earlier study[2] under the callout of Vendor B. The 2048- and 4096-bit versions follow the same design philosophy with the organization expanded to accommodate the increased capacity.

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2. "Reliability Evaluation of Programmable Read-Only Memories," Final Technical Report, RADC-TR-75-278, Hughes Aircraft Company for Rome Air Development Center, February 1976, (A022667).

The 2048-bit device is organized into 512 words of 4 bits each. The word decode is mechanized with 32 row decoders and 16 column decoders. If the chip is oriented with pin 1 at the upper left, the top row and right-most column contain extra fuses for testing. The 4096-bit device used in this study is organized as 512 words of 8 bits each, using 64 row decoders and eight column decoders. The extra test row is at the top, and two extra test columns are included in the extreme left and right positions.

VENDOR A (NICHROME)

This vendor has performed a major redesign of his PROM line since the earlier study. However, schematics for the new design were considered proprietary by the vendor and were not made available for this study.

VENDOR Y (AIM)

The circuit principles outlined for the 1024-bit device in the Final Report of an earlier study[2] under the callout of Vendor D are generally applicable to the larger capacity devices. Some differences exist in the chip enable and programming SCR control circuits. The 2048-bit device is organized into 512 words of 4 bits each. The word decode is mechanized with 32 row decoders and 16 column decoders. With pin 1 at the top, the two top rows contain extra test memory elements. The 4096-bit device is organized into 512 words of 8 bits each. The word decode is mechanized with 64 row decoders and eight column decoders. Again the top two rows are added for testing.

4. PROGRAMMING

In programming the devices to be used in the life tests, a careful effort was made to closely adhere to the vendor's programming recommendations, except when the programming amplitude was deliberately reduced to obtain long blow times. The pulse conditions are summarized in Table 3. The detailed programming procedures are contained in Appendix III. The pulse parameters were verified during actual device programming using a storage oscilloscope. Currents were monitored with a DC current probe. Since a slow mechanical printer was used to record the number of pulses required for programming, the programming rate was slow and low chip temperatures resulted. Reverification was performed after programming when the devices had returned to room temperature.

Occasional checks of the programming current waveforms (or voltage waveforms in the case of the devices programmed with a current pulse) were made. A DC current probe and a storage oscilloscope were used in an effort to detect any anomalous behavior. The waveforms seemed well behaved, and the current transients due to internal junction breakdowns experienced in an earlier study[2] were not observed. The impression was that significant design or processing improvements have been made since the earlier study. It may be that special techniques to avoid yield loss due to internal breakdowns, such as slowing the risetime or stair-stepping the pulse amplitudes, will be unnecessary in the future. It should be noted that slowing the rise time may be desirable for other reasons, such as control of the energy flow to the fuse and to assure blowing during the rise time, as some proponents recommend.

Several vendors have recommended significant changes in their programming procedures since the earlier study. The procedures of Vendor A are entirely different because of a major redesign. In 1975, Vendor B introduced a sawtooth pulse technique with the pulse amplitude stairstepped. According to the stairstepping recommendation, pulses 1 through 3 should

TABLE 3. PROGRAMMING PULSE CONDITIONS

Vendor	Device Capacity (Bits)	Program Pulsewidth*	Program Pulse Height*	Program Pulse Rise Time*	Auxiliary Pulse Height*	V_{CC} During Verification	V_{CC} During Programming
			(Chip Select Pin)		(V_{CC} Pin)		
X (Polysilicon)	1024	1 μs increasing linearly to 8 μs max. in 100 ms	15 V	200 ns	10 Volts	4.5 V	10 V
	2048				12.5 Volts	4.5 V	12.5 V
	4096				12.5 V	4.5 V	12.5 V
			(Output Pin)		(Enable Pin)		
B (Nichrome)	1024						
	2048	67 μs	23 V	60 μs	30 V	4.2 V	5.5 V
	4096	(Sawtooth)					
			(Output Pin)		(V_{CC} Pin)		
A (Nichrome)	1024						
	2048	100 μs	10.5 V	1 μs	12 V	4.2 V	12 V
	4096						
			(Output Pin)				
Y (AIM)	1024			400 ns (Measured with 200 Ω test resistor)			
	2048	7.5 μs	200 ma		None	4.2 V	5 V
	4096						

*The pulse, the width of which controls the programming time, is considered the programming pulse. The auxiliary pulse is an enabling pulse.

be at the lowest amplitude; 4 through 6 at an intermediate amplitude; and 7 through 9 at the highest amplitude. This multiple pulse technique is designed to optimize yield in commercial applications. However, the fuse is designed to blow in an abrupt, rather than gradual fashion, as in the case of those of Vendors X and Y, so that multiple pulses are not a necessity. Vendor B affirms that single pulse programming is a practical approach with their devices.

Current waveforms for programming Vendor X polysilicon fuse PROMs were studied. Voltage pulses were applied to both the V_{CC} and Chip Select pins. The programming current flows through the Chip Select pin to the fuse. Programming requires a long series of 1 to 8 μs pulses. Each successive pulse changes the resistance characteristics of the fuse by an increment. The current waveform through the Chip Select pin changes from pulse to pulse as shown in Figure 13. The reason for the changes in current waveform in this manner is unknown at this time.

Vendor X (Polysilicon) is at present introducing a major programming algorithm change. In an earlier change, the overprogramming time (time that the pulse train is applied after output voltage reversal is first detected) was increased to 500 μs. The latest revision calls for the following changes:

1. Overprogramming is now 2.5 ms of DC voltage, rather than 500 μs of pulsed voltage.
2. The pulse width is now initially 0.2 μs, increasing linearly to a maximum of 8 μs over a period of from 120 to 220 ms.
3. A constant down time of 10 μs between programming pulses is now specified, rather than a 50 percent duty cycle.
4. The data interrogation strobe should occur near the end of the down time.

These changes (Vendor X) were announced too late to be used in the life test programming.

The programming procedure recommended by Vendor Y (AIM device) remains unchanged, utilizing a 75 percent duty cycle pulse train. During the down time between programming pulses, a special verification procedure is instituted, involving the injection of a 20 mA interrogation current into the appropriate output pin and measuring the resulting output pin voltage. This

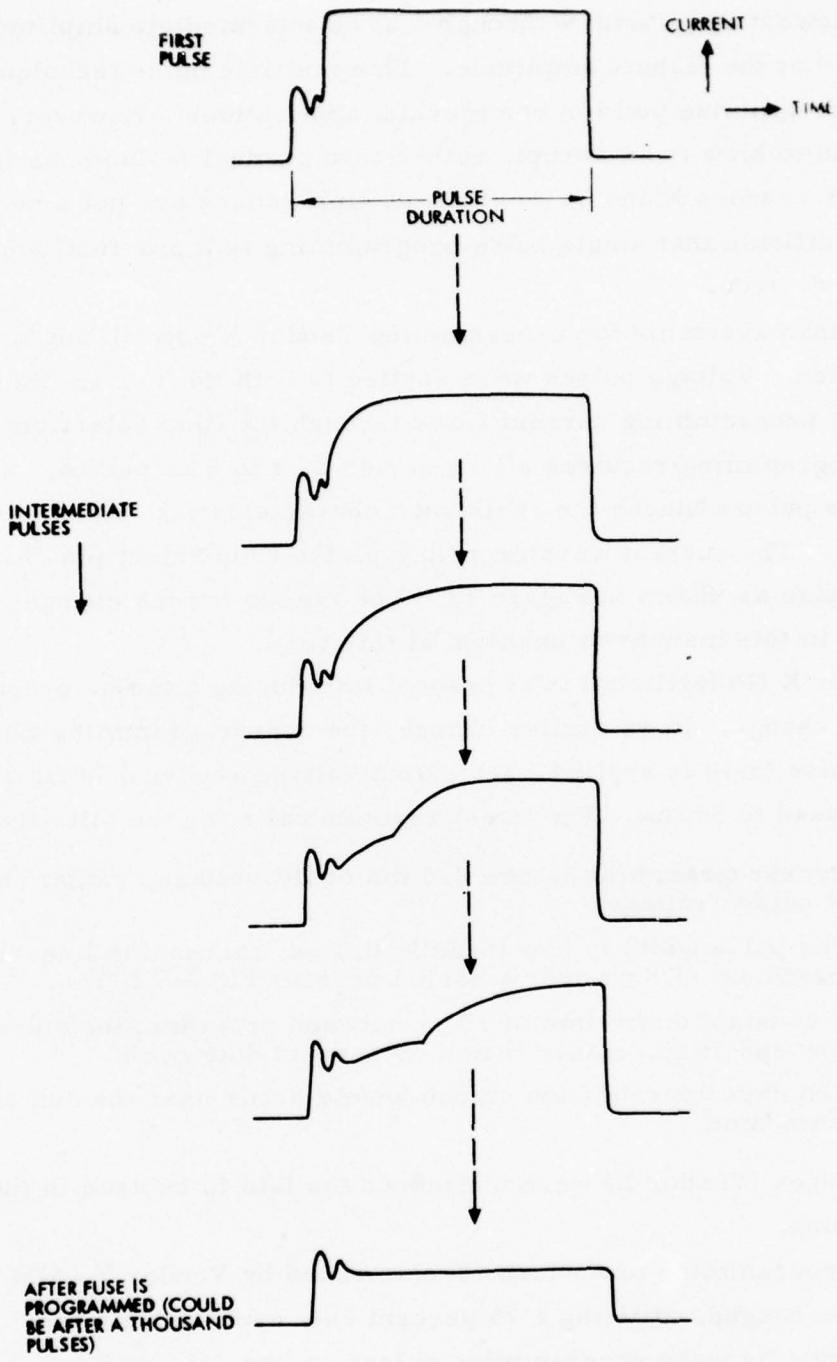


Figure 13. Programming current waveform, Vendor X (Polysilicon)

technique differs from the more usual technique of sensing the state of the programmable element through the on-chip sense circuitry in that this sense circuitry is bypassed and a nearly direct measurement of the element impedance is made. This permits detection of an incompletely programmed element whose presence might be concealed by the nonlinear characteristics of the sense amplifier.

A brief experiment was conducted to learn something of the programming characteristics of the nichrome link devices and their response to single pulse programming. Three samples from each (1K, 2K and 4 bit) capacity from both vendors A and B were used. The object of the experiment was to compare the programming yields for the application of a single pulse of 10 μs versus a single pulse of 100 μs. A sample size of 29 fuses for each attempt was scattered through the fuse matrix. It was found that a 10 μs pulse was adequate to successfully program nearly all of the devices. The exception was a 1024-bit device in which one fuse out of 29 refused to program in both the 10 μs and 100 μs attempts. Both of these fuses were found to lie on the same row in the matrix. Other fuses in the same row also refused to program in 100 μs. It appeared in this case that the problem lay in the row select circuitry.

In this very limited experiment it was shown that in the best of conditions, the fuses open very rapidly (less than 10 μs) but, if a defect exists, the programming time is extended considerably.

Table 4 presents the distribution of bits as a function of the number of pulses required to program them. Approximately ten 1K, ten 2K and five 4K devices were utilized for each of the four vendors. The figures in this table indicate that most of the bits can be programmed within the first ten pulses. The counting scheme devised did not provide sufficient resolution to categorize the bits below ten pulses. For the nichrome fuses programmed with vendor recommended methods, 87 percent of the fuses and 77 percent of the devices were programmed with 10 pulses. Those fuses that would not program within 10 pulses were distributed in all of the ten 2K devices of vendor B and in one 4K device of the same vendor.

TABLE 4. DISTRIBUTION OF NUMBER OF BITS PROGRAMMED WITH VENDOR RECOMMENDED METHODS AS A FUNCTION OF PULSES TO PROGRAM

Technology	Manufacturer	Device Capacity (Bits)	Number of Bits				
			Categories according to number of pulses required to program				
			1 to 9	10 to 99	100 to 999	1000 to 9999	Over 10,000
Nichrome	B	1K	6044	0	0	0	0
		2K	4631	3474	1785	337	13
		4K	10024	207	9	0	0
	A	1K	2560	0	0	0	0
		2K	5120	0	0	0	0
		4K	10240	0	0	0	0
Polysilicon	X	1K	0	0	6076	66	6
		2K	354	3717	1049	0	0
		4K	0	10	10225	5	0
AIM	Y	1K	2048	1002	22	0	0
		2K	3715	1405	0	0	0
		4K	6796	1395	0	0	0

Vendor X's 2K devices also behaved differently, but in the other direction, i.e., they tend to be programmed with fewer pulses than the 1K and 4K devices.

Although some bits refused to be programmed, the number of devices used in this study was insufficient for drawing conclusions on programming yield.

A survey was then made among PROM users throughout the industry concerning their experience with the devices. A questionnaire was circulated asking the part type and quantities used, percent chip usage, gle or multipulse programming, programming yield, burn-in and test experience, and field experience. A copy of the survey form is shown in Appendix I. The response is summarized in Table 5. Some additional test and failure information was collected, and is presented in the section under Burn-in and Life Tests.

It appears that the industry has been experiencing a programming yield of 90 to 98 percent for 1K and 2K devices. One source with a very limited number of devices programmed indicated that for one vendor the change of programming yield from multipulses to single pulse was from 80 percent to 50 percent. However, another vendor's product programmed by the same user showed an 89 percent yield for single pulse programming.

TABLE 5. USER PROGRAMMING YIELD DATA

Technology	Device Size (Bits)	Manufacturer*	Quality Level	Number of Parts Programmed	Chip Usage (Percent of Bits Programmed)	Single Pulse (S. P.) Multi-Pulse (M. P.)	Programming Yield (Percent of Parts)
Nichrome	256	C	Commercial	10,000	50	M. P.	90 to 98
	1K	D	38510-B Equivalent	50	36	M. P.	86
		A	Commercial	5,000	50	M. P.	90 to 98
			Commercial	5,000	50	M. P.	90 to 98
		B	Commercial	175,000	25	M. P.	86
	2K	B	38510-B Equivalent	117	34 to 43	M. P.	75
		B	Commercial	22	34 to 43	M. P.	91
		A	Commercial	500	50	M. P.	90 to 98
		A	Commercial	29	50	S. P.	89
		B	Commercial	30	50	S. P. M. P.	50 80
Polysilicon	1K	X	Commercial	170,000	Unknown	M. P.	97
	2K	X	Commercial	60	50	M. P.	90
AIM	512	Y	38510-B Equivalent	6,120	25	M. P.	90 to 95
	1K	Y	Commercial	400,000	Unknown	M. P.	96
Titanium Tungsten	1K	G	Commercial	190,000	Unknown	M. P.	90

*C = National
D = Fairchild
G = T.I.

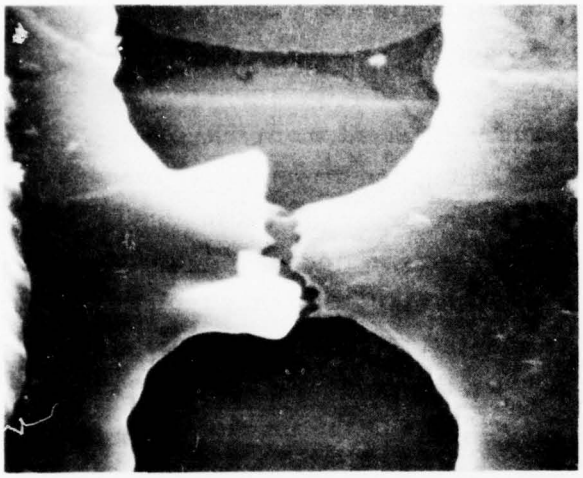
5. MEMORY ELEMENT PROGRAMMING MECHANISMS

POLYSILICON FUSE PROGRAMMING MECHANISM

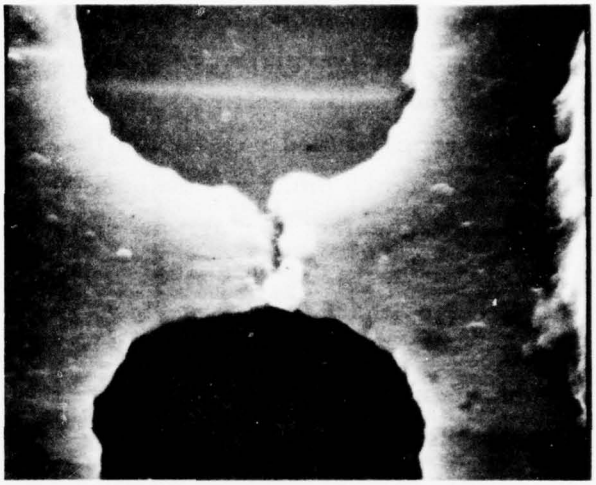
The structure of the memory elements in the polycrystalline fuse PROM is similar to nichrome fuses, as was described in Section 2. Due to the absence of overglass passivation on the polysilicon fuse element and a thickness more than ten times greater than the nichrome film, the appearance of a programmed polysilicon fuse is considerably different from that of a programmed nichrome fuse. When the programming conditions recommended by the manufacturer are used, most of the fuses are programmed in about 2 ms. Examination of these fuses in a scanning electron microscope (SEM) revealed that they appear to have been melted in the middle. They typically have two rounded lumps near the middle, as shown in Figure 14a, with a gap on the emitter (positive) side of the lumps. When the programming current is reduced to obtain long fusing times, the appearance of the fused gaps is different. Several small lumps and a narrower gap occur, as shown in Figure 14b-d. The change from a few large lumps to several small lumps occurred between fusing times of 12 and 29 ms on the 1024-bit sample that was tested, as shown in Figure 14.

Under reduced programming current, the maximum fusing time observed was 17.4 s. However, a few fuses had not blown after the maximum time allowed, 40 seconds. After etching away the oxide, these unblown fuses did not show any change in appearance of their surfaces in the SEM but did appear darker in the middle of the fuse. This may have been caused by etching away of the SiO_2 under the fuses that were heated but not fused, therefore, a change in the polysilicon-SiO_2 interface may result from that heating. Unprogrammed fuses appeared uniform across the fuse.

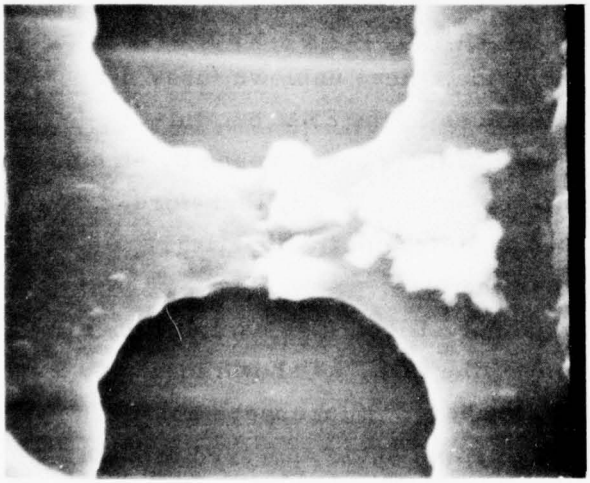
The use of a glass etchant on programmed polysilicon fuse samples does not remove the lumps formed near the middle of the fuse, as shown in Figure 15. Even the smallest lumps on this slowly blown fuse were not changed by the selective oxide etchant, although some oxide appeared to have



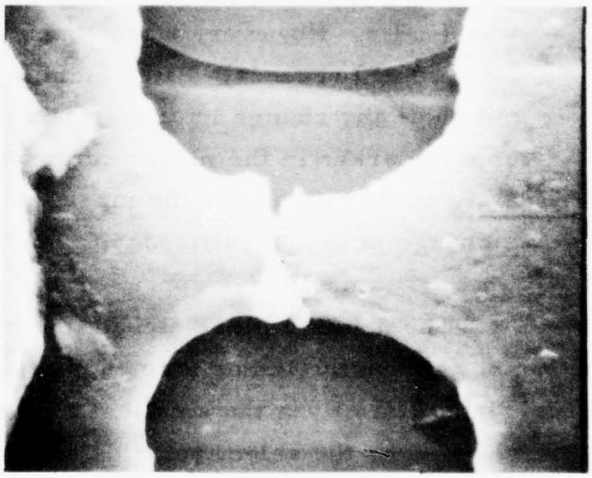
a. Fusing time = 1.7 ms.



b. Fusing time = 12 ms.

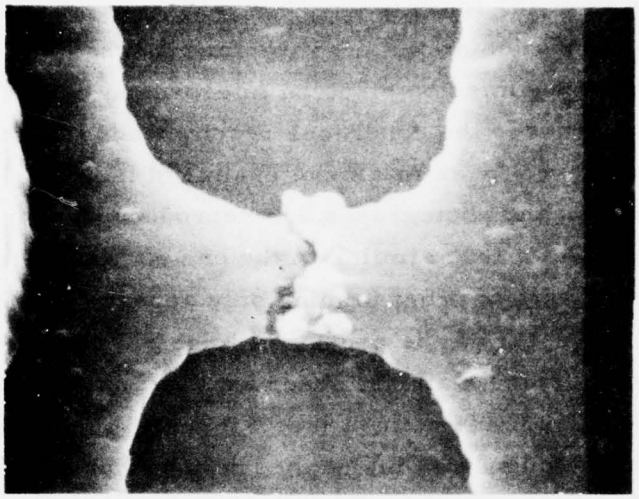


c. Fusing time = 29 ms.

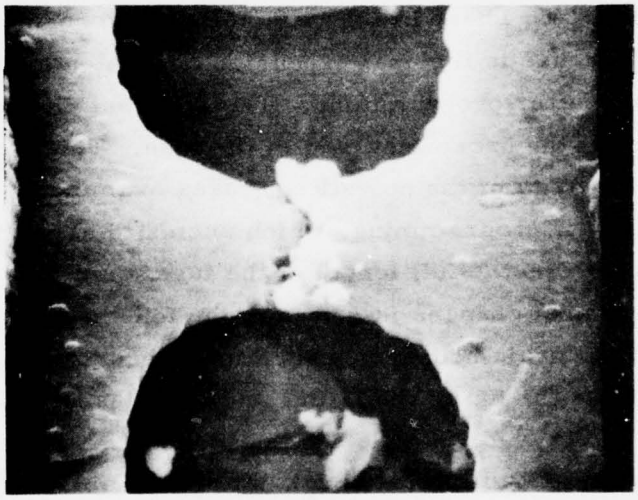


d. Fusing time = 320 ms.

Figure 14. Scanning electron microscope photos of programmed polysilicon fuse PROM elements, sample D. The overglass and exposed oxide were etched off the device before the photos were made except for photo b. (Disregard the pieces of dirt on the right side of that photo.) The actual minimum widths of the fuses shown is about 2 μm.



a. Before etching.



b. After etching.

Figure 15. Effect of etching with buffered HF on programmed polysilicon fuse, sample D. (Fusing time 11.7 seconds; actual width of fuse at center 2 μm)

been removed from the gap. Therefore the lumps must be Si, not oxide. Their sizes appear commensurate with the polysilicon lost from the gap and other thinned areas of the fuses.

Additional information on the programming mechanism of polysilicon fuses was obtained from transmission electron microscope (TEM) photographs of a PROM programmed under the conditions recommended by the manufacturer.* A summary of the seven fuses that were examined in detail is presented in Table 6 and four of the photographs are reproduced in Figures 16-19. Figure 16 shows a blown fuse similar to the one shown in the SEM photo of Figure 14a. The effects of programming only appear near the neck of the fuse. The material in the gap is presumed to be SiO_2 formed before and during programming, since some material observed there in the SEM photos was removed by a selective oxide etchant (see Figure 15). There may also be some thin silicon extending into the gap. The fuse link shown in Figure 17 also has changed only at the neck. Only one large lump appears there and it is directly over the possible gap in the fuse. A narrow crack in the grey gap region is visible in the original negative on both sides of the lump.

The crack in the thin region of a fuse link is more visible in TEM photo number 73, Figure 18. These cracks are believed to result from the stress caused by the difference in thermal expansion coefficients of SiO_2 and the Si chip during cooling after programming. The apparent physical discontinuity in this fuse is not at the narrowest part of the fuse. This is the situation observed in the majority of the polysilicon fuses examined. Also typical is the extensive effect of programming, which seems to have thinned and/or produced grain growth over the full length of the fuse. Another example of extensive programming changes is shown in the fourth TEM photo, Figure 19. Note the longitudinal grain boundary where transverse twins terminate on the end of the fuse at the top of the figure and the cresent - shaped dark region on the other end of the fuse. The latter is a common feature in the TEM photos, as indicated in Table 6, although not discernable in the other photos

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*The sample was prepared by M. Fukuda and O. Manuel and analyzed under the direction of W.K. Jones of the Charles Stark Draper Laboratory.

TABLE 6. SUMMARY OF TRANSMISSION ELECTRON MICROGRAPHS OF POLYSILICON FUSE LINKS PROGRAMMED UNDER CONDITIONS RECOMMENDED BY THE MANUFACTURER

Photo Number	Area Affected	No. of Lumps	Crack in Gap?	Crescent on + Side?	Recrystal-lization Structure?	Comments
72	large	1	yes	yes	yes	
73	large	1	yes	yes	yes	
74	large	1	yes (short)	yes	yes	
75	large	1	yes	yes	yes	
77	small	2	no	no	no	
78	small	1	yes	no	no	Lump at center of gap
79	large	1	no	yes	yes	Foreign particles present

Figure 16. TEM photo 77.

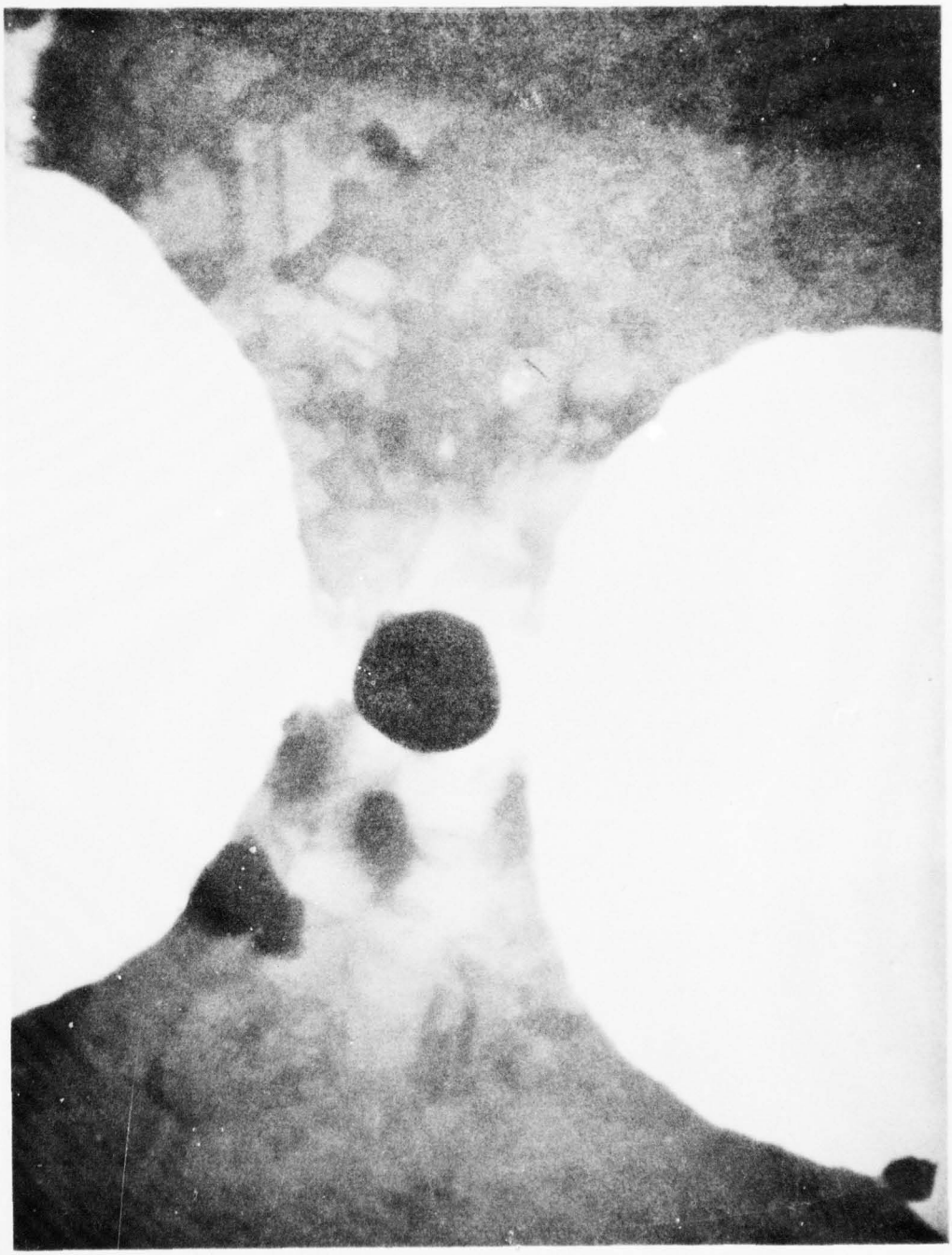


Figure 17. TEM photo 78.

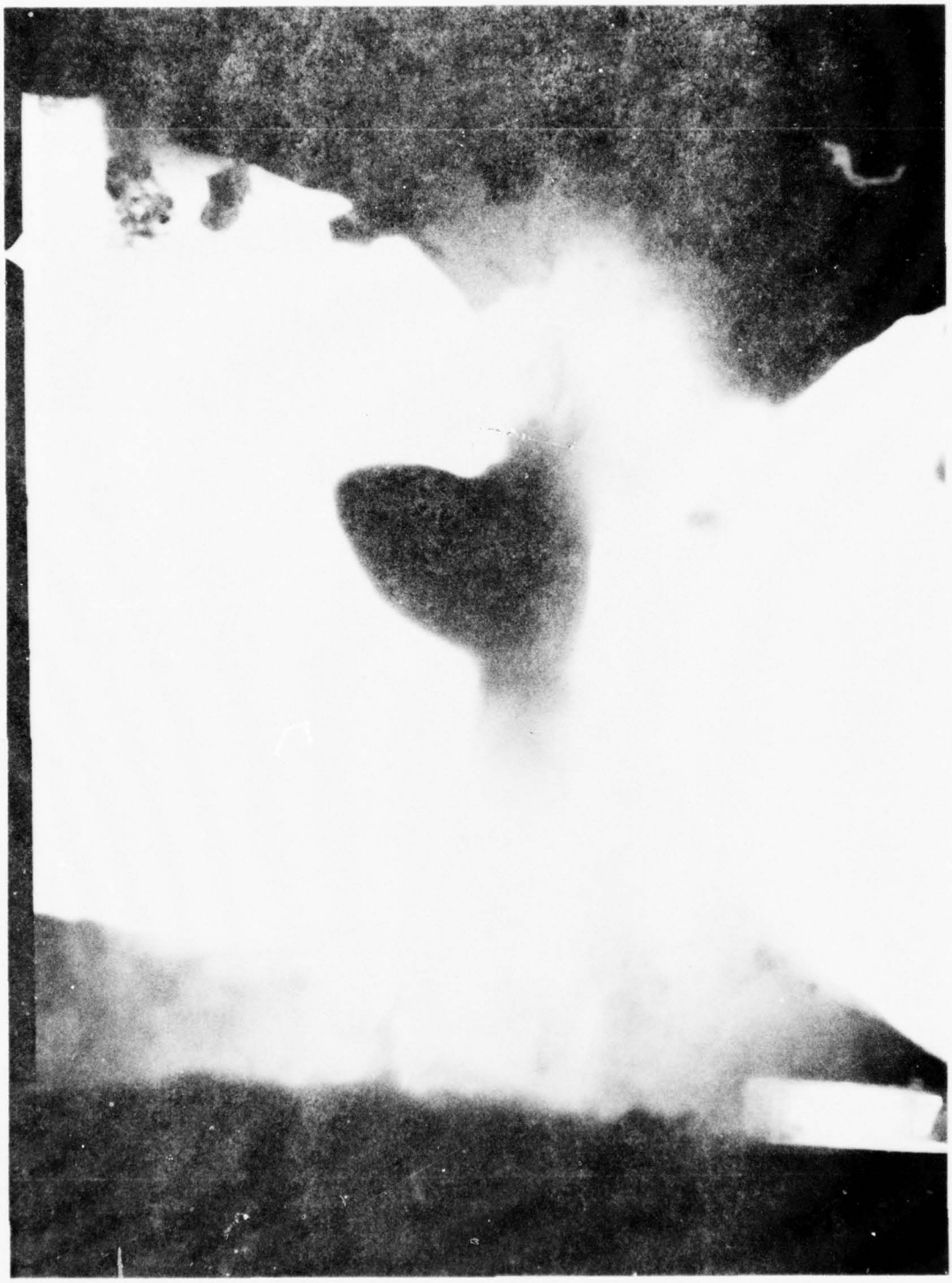


Figure 18. TEM photo 73.

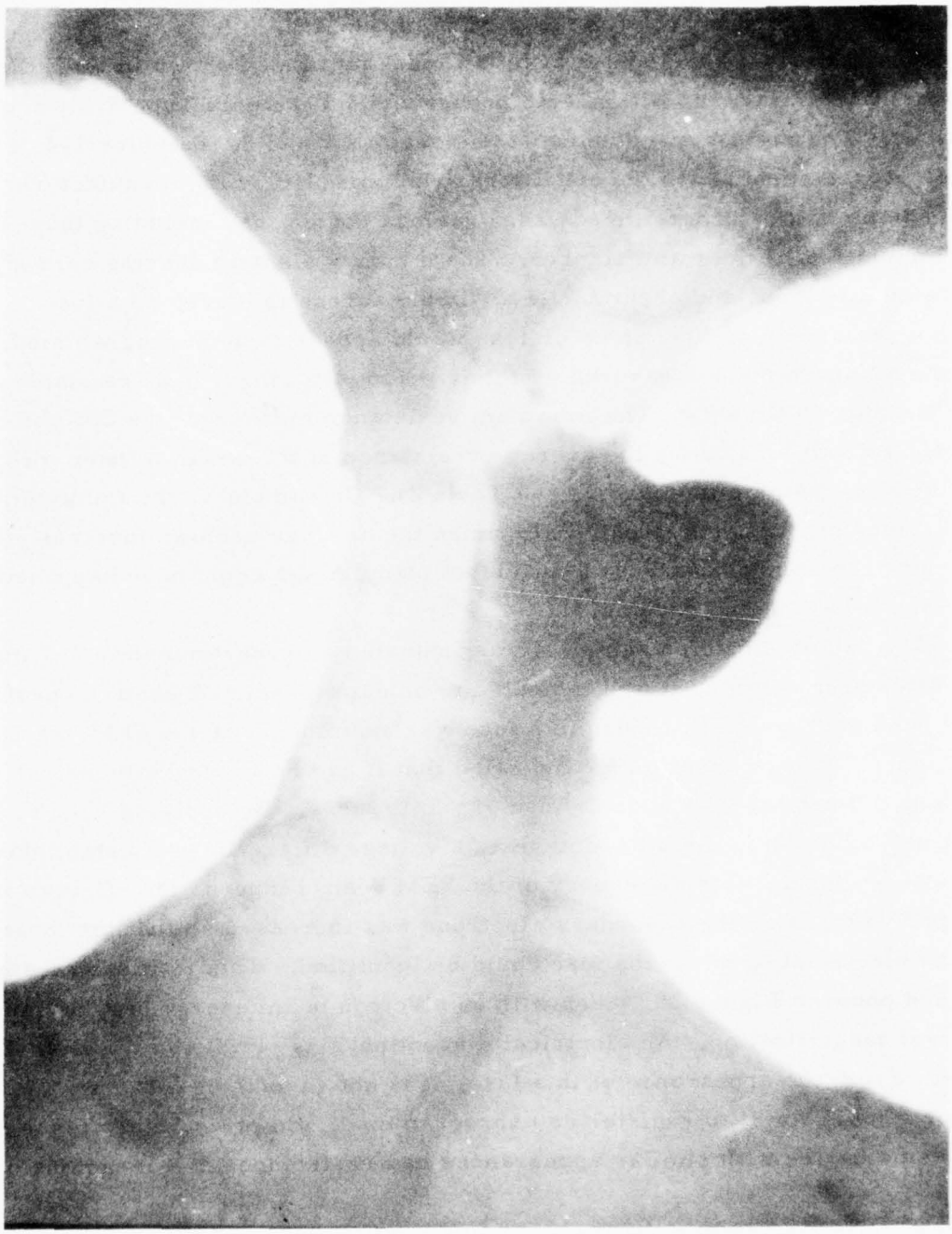


Figure 19. TEM photo 74.

shown here. There are some short cracks in the "gap" in Figure 19 but they do not extend the full width of the fuse as does the one in Figure 18. In all four of the TEM photos, the physical "gap" (where there is no sign of polysilicon) is surprisingly narrow at its minimum width, although thinning has usually occurred over a large portion of the fuse.

The electrical resistances of blown fuses (not those shown in the TEM photos) were measured with needle probes and a Tektronix Type 576 Curve Tracer. The results are summarized in Tables 7 and 8. Samples 1-4 were programmed under the conditions recommended by the manufacturer and sample D was programmed under various conditions, including those recommended by the manufacturer. The memory element sensing current is nominally 2 mA and about 2 V is available across the fuse, so a fuse with a resistance of 1000 ohms or less would appear to be unprogrammed. Of the 57 blown fuses measured on the five samples, three had resistances of less than 1000 ohms. The minimum resistance measured was 224 ohms, which is about four times the average resistance of the unblown fuses measured on the same sample (number 3, see Table 2). On sample 2, the minimum resistance of 275 ohms is only 2.75 times the average unblown fuse resistance. The low resistances are unexplainable as many things could have happened during de-lidding and probing.

The 760 ohm fuse on sample 4 was indicated as programmed in 3.7 ms but after programming it was indicated to be unprogrammed when the device was read out (verified). When this fuse was examined with the SEM, as shown in Figure 20, prominent lumps indicated that it had been programmed but etching did not reveal a well-defined gap in the fuse. By applying V_{CC} to the chip and addressing the bit of interest, a voltage difference was established across the fuse. With the energy of the SEM beam reduced, the effect of the circuit voltages on the secondary electrons was increased so that the location of the electrical break in the fuse could be identified. This is illustrated by the second photo in Figure 20, taken with an electron beam energy of 2 keV and a lower magnification. An electrical discontinuity is visible on the right-hand side. From the appearance of this fuse, it is not surprising that its resistance is low enough for it to register as unprogrammed. However, other fuses on the same device with similar appearances had resistances of 4 megohms or larger.

TABLE 7. RESISTANCES OF BLOWN FUSES ON 1024-BIT POLYCRYSTALLINE SILICON PROM DEVICES

Programming Method	Sample Designation	Condition	Number of Fuses Measured	Minimum Resistance (Ohm)	Next to Minimum Resistance (Ohm)	Maximum Resistance (Ohm)
Manufacturer's Recommended Method	1	As blown	6	1.8×10^3	$>10^8$	$>10^9$
	2	As blown	5	275	7×10^3	$>10^9$
	3	Etched*	7	224	1.2×10^3	3.2×10^6
	4†	Etched*	8	760**	1.2×10^6	$>70 \times 10^6$
		Fusing time:	1.8 - >600 ms	3.7 ms	Unrecorded	>10 ms
Various Programming Currents	D	Etched*	31	78×10^3	10^6	$>4 \times 10^9$
		Fusing time:	1.7 ms - 17 s	83 ms	17 s	1.7 ms - 15 s

*For 1 minute in buffered HF to remove overglass and oxide for SEM analysis.

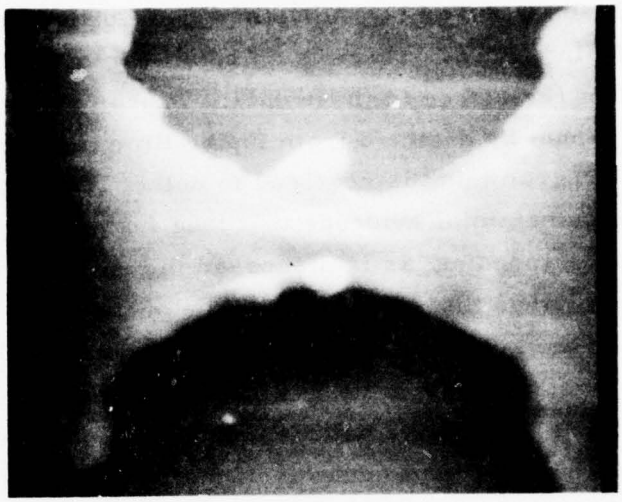
**Verification after programming indicated not blown. SEM analysis indicated only partially blown.

†See Table 8 for more details on sample 4.

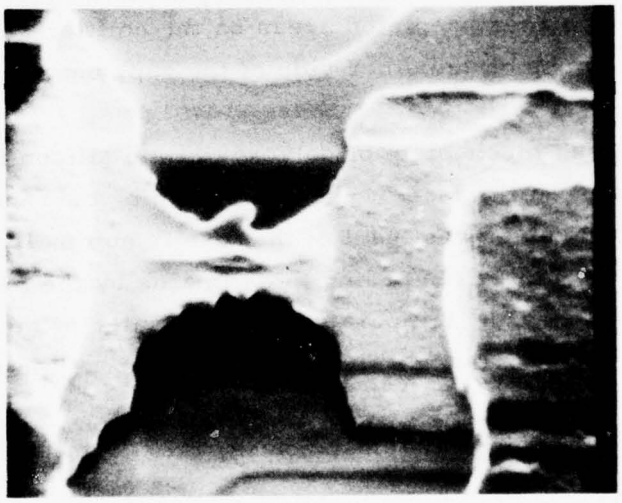
TABLE 8. OBSERVATIONS ON BLOWN POLYSILICON FUSES, 1024-BIT PROM, SAMPLE 4

Fuse Location				Appearance in SEM*			
Bit	Row	Column	Fusing Time	Without Bias	Voltage Contrast	Resistance* (Ohm)	Comments
1	31	7	>>10 ms	Continuous	Continuous	4M	Poorly blown
1	23	7	>10 ms	Small gap	---	>70M	Good fuse
1	22	6	4.6 ms	Continuous	---	>7M	Breakdown @ +0.5V, -1V observed when measuring resistance. Poorly blown.
3	28	4	>10 ms	Continuous	Discontinuous	~30M	Poorly blown
4	26	2	3.7 ms	Continuous	Discontinuous	760	Not blown when checked after programming. Incompletely blown.

*After sample was etched for 1 minute in buffered HF to remove overglass and oxide.



a. Normal SEM, 20 keV.



b. Voltage contrast, 2 keV.

Figure 20. Incompletely blown fuse on polycrystalline silicon PROM sample 4. (Fusing time 3.7 ms)

The fusing time data presented in Table 7 for samples 4 and D indicate that open circuit fuses (resistances $>10^7$ ohm) were produced with almost the full range of fusing times. There is no significant correlation between fusing time and fuse resistance in these data. Therefore, low resistance polysilicon fuses cannot be detected from fusing time measurements and verification after programming is required to detect such faults. However, there is a little circumstantial evidence that long fusing times are undesirable from the reliability standpoint, as is discussed in Section 6 of this report.

The polysilicon lumps that form on one side of the gaps of programmed fuses are always on the side connected to the column bus. (The other end of each fuse is connected to the emitter of the npn transistor in each memory cell.) The column bus is negative with respect to the emitter during programming (and sensing), so the formation of the lumps appears to be influenced by the electric field across the fuse during programming. This would be expected if the power dissipated in the fuse during programming is sufficient to heat the polysilicon to its melting point, 1420°C, since positive ions are responsible for viscous flow and diffusion in liquid metals.[3] Melting is also indicated by the appearance of the fuses in the SEM and TEM, which usually show thinned, depleted areas on the emitter side of the gap and smoothly rounded lumps on the other side of the gap, near the narrowest part of the fuse link.

The programming mechanism of polycrystalline silicon fuse PROMs first involves joule heating of the fuse by the programming current, for which the current density at the narrowest part of the fuse is nominally 30 mA/(2 μm x 0.35 μm) = 4×10^6 A/cm^2. According to estimates by the manufacturer,[4, 5] this is sufficient to raise the temperature of the center of the fuse to about 1400°C and melt the polysilicon. The surface tension of the molten silicon

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[3] W. Jost, Diffusion in Solids, Liquids, Gases, third printing (Academic Press, NY, 1960), p. 470.

[4] G. Parker, J. Cornet, W. Pinter, "Reliability Considerations in the Design and Fabrication of Polysilicon Fusable Link PROMS," Proc. IEEE 1974 Reliability Physics Symposium (IEEE, NY, 1974), pp. 88-89.

[5] B. Pascoe, "Polysilicon Fuse Bipolar PROMs", Intel Reliability Report RR-8 (Intel Corp., October 1975).

forms it into one or more droplets there, leaving thinned regions on both sides of the center. Simultaneously, migration of Si occurs under the influence of the electric field, which acts upon the positive ions in the molten Si, and the thermal gradients across the fuse. On the negative side of the droplets, migration under both influences occurs from the droplet, toward the cool end of the fuse, which tends to extend the droplets in that direction. However, on the positive side, migration of molten Si under the electric field influence occurs toward the central droplets from the thin, now hotter area between the droplets and the emitter contact. Silicon also migrates from that region toward the cooler emitter contact under the influence of the thermal gradient, which may produce the crescent of thicker material observed in the TEM photos on the emitter ends of most of the fuses. The consequent depletion of Si between the emitter contact and the central droplets soon results in opening the fuse link there, which interrupts the electric current. The polysilicon then cools rapidly as a result of thermal conduction to the underlying SiO_2 and Si and to the metallization at the ends of the fuse.

The final opening of the thinned polysilicon fuse link may result from the surface tension of the liquid polysilicon sheet, as appears to be the case for nichrome fuse links, from formation of voids by Si migration, or from oxidation of the remaining polysilicon. No artifacts similar to those seen in nichrome fuse gaps, such as periodic fingers or droplets,[6, 7] are seen here so the physical effects of surface tension and viscosity do not appear to play as significant a role with polysilicon fuses. Chemical change by oxidation is not important for NiCr fuses, which are protected by an overglass layer. Although the polysilicon fuse PROMs that were tested had a phosphosilicate glass passivation layer (see Section 2), openings are etched

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[6] G. Kenney, W.K. Jones, R. Ogilvie, "Fusing Mechanism of Nichrome-Linked Programmable Read - Only Memory Devices," Proc. IEEE 1976 Reliability Physics Symposium (IEEE, NY, 1976), p. 164.

[7] G.B. Kenney, "The Fusing Mechanism of NiCr Resistors in Programmable Read - Only Memory Devices," BS-MS thesis submitted to Dept. of Materials Science and Engineering, MIT, June 1975.

in this layer over the chip bonding pads, as usual, and also over every polysilicon fuse element. The latter openings were reportedly added after fusing difficulties were encountered.

Removing the overglass would have at least two benefits: Less energy would be required to heat the fuse, since less mass is in contact with it, and the free surface would allow fast migration of the polysilicon material to open the desired gap in the fuse. In addition, oxidation could occur. The SEM photos of etched polysilicon fuses (Figure 15 et al.) show that some SiO_2 does form at the gap of these fuses, so oxidation appears to take place in the last phase of programming these fuses. However, one supplier of this type PROM, whose parts were not included in this study, was said to have successfully used nitrogen to fill the package instead of oxygen, so oxidation is probably not essential to the programming of polysilicon fuses. The physical changes due to surface tension and void formation will suffice if oxidation does not occur first. (Note that formation of SiO_2 at the gap would provide protection against shorting by particles in the package, a possible advantage for reliability.)

AIM MEMORY ELEMENT PROGRAMMING MECHANISM

The avalanche-induced migration (AIM) memory element is an npn transistor without a base connection, as described in Section 2. Programming is effected by applying pulses of 200 mA and 7.5 μs long across the transistor, with the pulse polarity such that the e-b junction is reverse biased and the b-c junction is forward biased. After each programming pulse, the element is sensed with a current of 20 mA to see if the e-b junction is shorted. In the tests conducted, less than 32 pulses were required for programming under the conditions recommended by the manufacturer. After the sense pulse indicates the location is programmed, four more 200 mA pulses are applied, according to the manufacturer's recommendations, in order to insure permanent shorting of the e-b junction. (The use of post-programming pulses sometimes results in shorting of the b-c junction as well, which disables the device. Thus additional pulses might decrease the programming yield).

After the memory elements have been programmed, no evidence of programming is detectable with either visible light or electron beam (SEM) micrography.[8] However, after the glass and aluminum films are removed by chemical etching, lumps are seen on the emitter contacts. In the earlier evaluation of PROMs by Hughes Aircraft Company for RADC,[9] these artifacts were shown as light spots in SEM and optical photos. SEM photos made during this program clearly show these light spots to be lumps of etch-resistant material, 1-2 μm in diameter, as shown in Figure 21. The dark features in the emitter contact window are normal Al-Si alloying pits. We found lumps when either NaOH solution or a mixture of phosphoric and nitric acids was used to remove the Al metallization.

Energy dispersive analysis of Xrays (EDAX) in the SEM indicated the presence of Si and perhaps Al in these lumps. EDAX of the aluminum emitter contacts on programmed junctions after only the passivation glass was removed failed to show any Si-rich areas in the Al contacts.

A similar lump on an AIM emitter contact is shown in the report by Brockhoff.[8] These lumps resemble the "sintering residues" that were found by McCarthy[10] on (100) Si surfaces after removing the Al film by etching. The electron diffraction pattern of one of those particles was reported to show a crystalline structure close to that of Si.

The white lumps on the AIM devices appear to be caused by diffusion of Si into the Al film that contacts the emitter during programming. The resulting Al-Si mixture is quickly quenched at the end of the programming pulse, resulting in a Si-rich region that etches slower in an Al etchant than does the surrounding Al. (The Si from the alloying pits probably forms a

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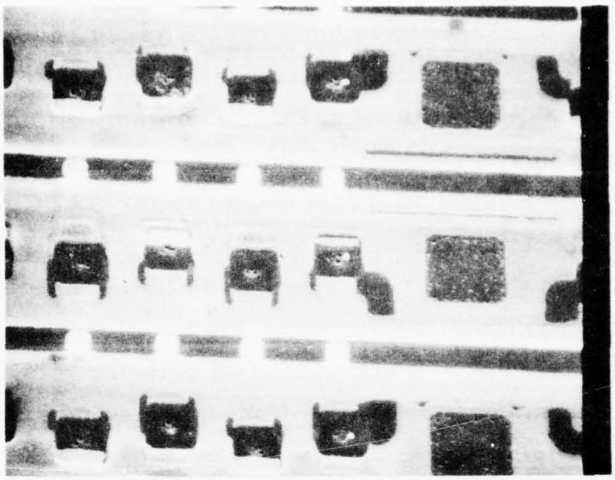
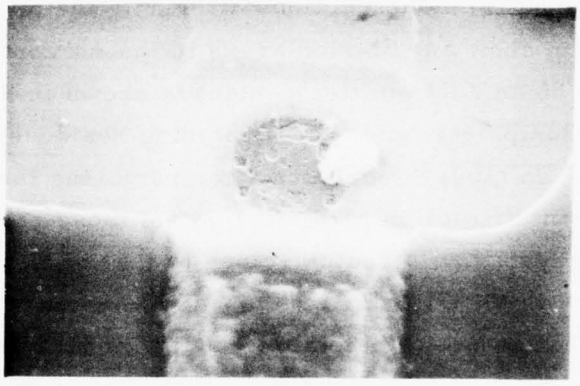
[8] W. R. Brockhoff, "Electrically Shorted Semiconductor Junctions Utilized as Programmable Read - Only Memory Elements," Proc. IEEE 1976 Reliability Physics Symposium (IEEE, New York, 1976), p. 202.

[9] T. M. Donnelly et al., "Reliability Evaluation of Programmable Read - Only Memories (PROMs)," report RADC-TR-75-278 (February 1976).

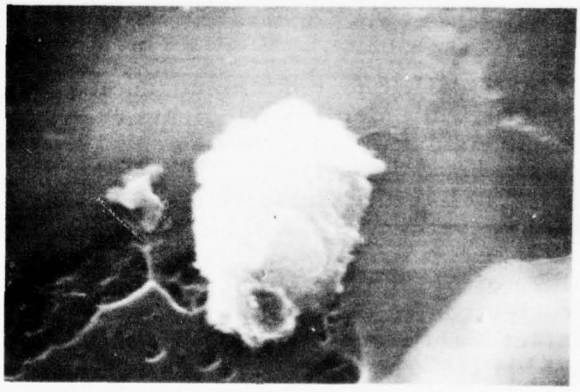
[10] J. McCarthy, "Failure of Aluminum Contacts to Silicon in Shallow Diffused Transistors," Microelectronics and Reliability 9, 187 (1970). See also C. J. Kircher, "Contact Metallurgy for Shallow Junction Si Devices," J. Appl. Phys. 47, 5394 (1976).



a. Partially programmed device, all Al metallization removed.



b. Bottom Al metallization intact.



c. Close-up of b. Lump ~2 μm in length.

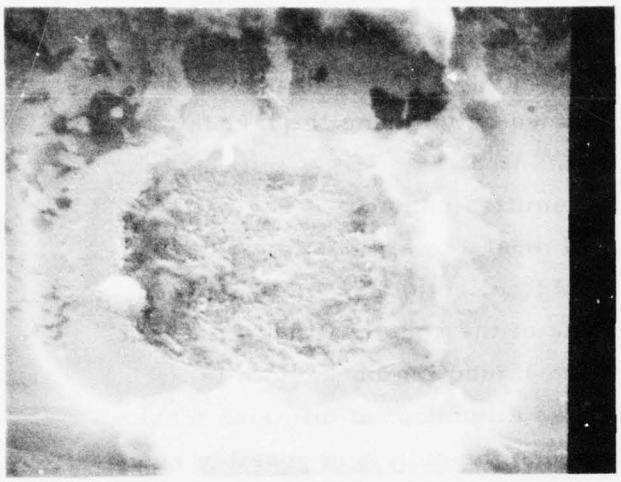
Figure 21. Etch-resistant lumps on emitter contacts of AIM memory elements.

dilute solution in the overlying Al during the extended contact sintering step and probably does not significantly change the etch rate.) When memory elements were programmed under abnormal conditions so that many pulses were required, the size of the lumps did not change, as shown in Figure 22. This indicates that the lumps are probably formed only during the last few pulses that permanently short the e-b junction.

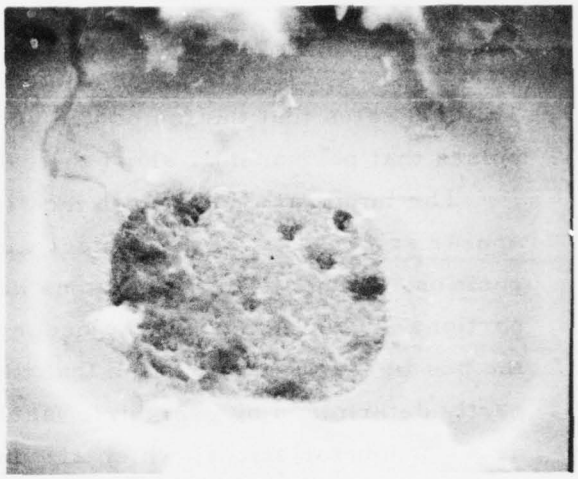
The lumps are uniform in location on the emitter contacts. They all appear at the edges of the contact windows and most are at the same relative position. Contacts in the columns next to the Al collector bus lines between portions of the memory array occur on the side of the contact window nearest the bus lines. This indicates that the point of e-b junction breakdown is partly determined by geometric factors, such as alignment of diffusion masks or Al conductor strips, which are uniform across the chip (and possibly even across the entire wafer from which the chip came).

Additional programming artifacts are revealed when the memory chip is sectioned by metallurgical techniques. Special sample alignment equipment was used to obtain sections closely parallel to the rows of memory elements. Figure 23a is a photograph of a portion of a 90^{o} section along a row of programmed memory element transistors. Since the transistors are stagggered in location on the surface of the chip (see Figure 21), only every second transistor appears in any one section. Note the aluminum-colored "fingers" extending diagonally downward from the edges of the emitter contacts toward the corners of the base-collector junctions. The fingers are about 0.5 μm in diameter with a circular cross section, as shown in the 6 degrees section, Figure 23b. The 30 degrees section in Figure 23c shows that the fingers cross the emitter-base junction below the surface of the chip. These fingers were not found on unprogrammed devices that were also sectioned.

The formations shown in Figure 23 are similar to those revealed in the 2^{o} sections presented by Brockhoff.[8] He described these programming artifacts as aluminum filaments and likened them to the white spears that have been seen on the surfaces of semiconductor devices between Al contact

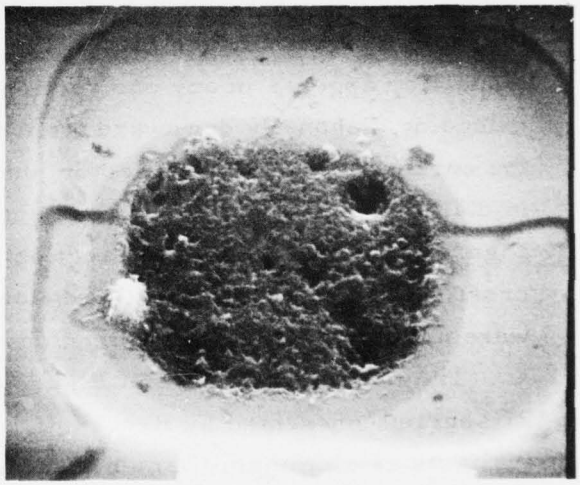


a. 24 ±8 pulses.



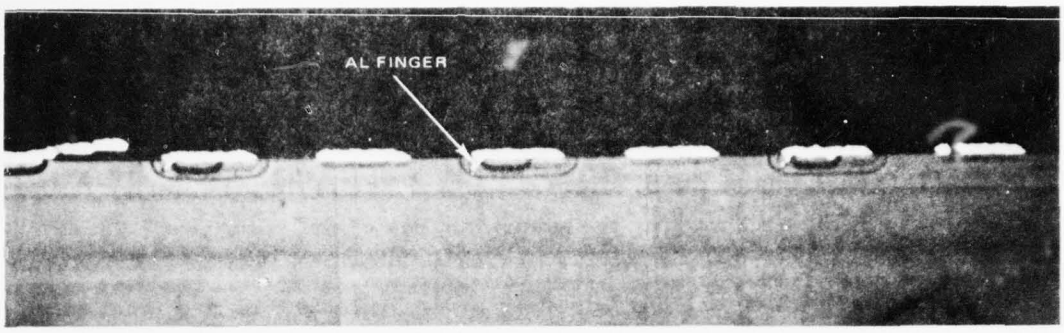
b. 520 ±8 pulses.

c. 6152 ±8 pulses.

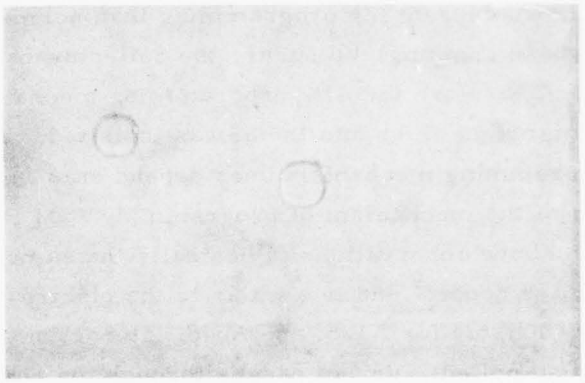


d. 57,352 ±8 pulses.

Figure 22. Programming artifacts on AIM memory elements for various pulses required to program (emitter contact windows ~5.5 μm wide).



a. 90 degrees section (e-b junction ~ 1.5 μm below silicon surface and b-c junction ~ 2.5 μm below surface).



b. 6 degrees section.

c. 30 degrees section.

Figure 23. Optical microphotos of sections through AIM PROMs with all locations programmed.

areas after overstressing. Aluminum spears have been produced[11] by simply heating specimens of an Al metallized transistor test pattern in a furnace at 560°C or higher for 20 seconds or longer. At 550°C, none were produced after 10 minutes. The reaction proceeded most rapidly in a direction parallel to the (111) surfaces of the Si slices. The surface of the AIM device is the (100) plane of Si, as shown by the square shapes of the alloy pits[12] in Figures 21 and 22. The Al fingers appear to extend approximately parallel to (111) planes, which are 54.7 degrees away from (100) planes, just as do the spears.

In the earlier evaluation of PROMs by Hughes,[9] it was reported that fabricating AIM PROMs with a diffusion barrier film (Ti-W) between the Si emitter contact and the Al metallization resulted in devices that required at least 50 percent more current for programming than normal. When programming (emitter-base shorting) did occur, the collector-base junction was also destroyed. Therefore the AIM programming mechanism apparently was changed when migration of Al into the Si was inhibited. This implies that the normal programming mechanism does depend on Al migration.

The explanation of the mechanism of programming AIM PROM elements that accounts for the above observations is basically the same as that presented in the earlier report[9] and is similar to the electro-thermomigration theory developed by Christou for Al-Si and Au-Si interactions.[13] When the programming pulse is applied, current passes through the reverse biased emitter-base junction and a hot spot forms at the junction where the electric field is strongest, near a corner of the emitter region. After joule heating raises the temperature of the nearby Si to over 560°C, rapid migration of Al occurs from the emitter contact to the hot spot under the influence of the

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[11] T.E. Price and E.A. Berthoud, "Aluminum spearing in silicon integrated circuits," Solid - State Electronics 16, 1303 (1973).

[12] E. Philofsky and E.L. Hall, "A Review of the Limitations of Aluminum Thin Films on Semiconductor Devices," IEEE Trans. On Parts, Hybrids, and Packaging PHP-11, 281 (1975).

[13] A. Christou, "Electro-thermomigration in Al/Si, Au/Si interdigitized test structures," J. Appl. Phys. 44, 2975 (1973).

thermal gradient and the concentration gradient. If localized melting of the Al and/or an Al-Si alloy occurs, as is likely since the Al-Si eutectic melts at 577°C, the electric field will also assist diffusion of Al since positive metal ions are responsible for diffusion in liquid metals.[3] Simultaneously, Si diffuses out of the emitter region into the Al contact because of the concentration gradient, replacing the Al that diffused to the hot spot. (Melting of Si is probably not necessary since Si diffuses rapidly in Al at temperatures above 500°C.[12]) After the junction is shorted by the Al "finger", the power dissipation drops and the region cools by conduction to the surrounding silicon. This rapid cooling quenches the Al and Si, preventing formation of equilibrium phases and preserving the inhomogeneous structures observed as white lumps on the emitter contacts and Al fingers in the sections.

NICHROME FUSE PROGRAMMING MECHANISM

The nichrome fuse PROM has been studied by many investigators. The phenomena involved and the appearances of programmed nichrome fuses have been adequately reported elsewhere, especially in the previous report.[9] The most significant recent contribution in this area is the work of Kenney, Jones, and Ogilvie.[6, 7] Additional insights are provided in the recent paper by Davidson et al.[15]

A technique for preparing samples of nichrome fuse PROMs for analysis by a transmission electron microscope (TEM) was developed by Jones.[14] This enables examination of undamaged fuses at high magnification and high resolution. Photographs of fuses obtained by this technique have been published.[6, 7, 15] Two of those photographs[7] are included in this report.

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[14] W. K. Jones, "Plasma Etching as applied to Failure Analysis," Proc. IEEE 1974 Reliability Physics Symposium (IEEE, NY, 1974), p. 43.

[15] J. Davidson, J. Gibson, S. Harris, T. Rossiter, "Fusing Mechanism of Nichrome Thin Films," Proc. IEEE 1976 Reliability Physics Symposium (IEEE, NY, 1976), p. 173.

Figure 24 shows the appearance of one type of nichrome fuse link, which is used by vendor A. The metal remaining in the gap is in the form of filaments with periodic aberrations in width along their lengths. The spacings between filaments is quite uniform. Segregation of the constituents was detected, with more Cr near the ends of the longer and wider filaments on the negative side of the gap and more Ni near the ends of the smaller filaments on the positive side of the gap. Also present in the gap is a film of Ni-Cr spinel (Cr_2NiO_4), which contains some round voids. (The chemical compositions were determined by non-dispersive x-ray spectroscopy on a scanning TEM and by electron diffraction from areas about 50 nm in diameter). The breaks in the NiCr filaments occur near the end of the fuse link away from the emitter of the memory element transistor. Thus the breaks are near the positive end of the fuse (see the circuit diagram in the previous report [9]), which is also the location of the break in polysilicon fuse links.

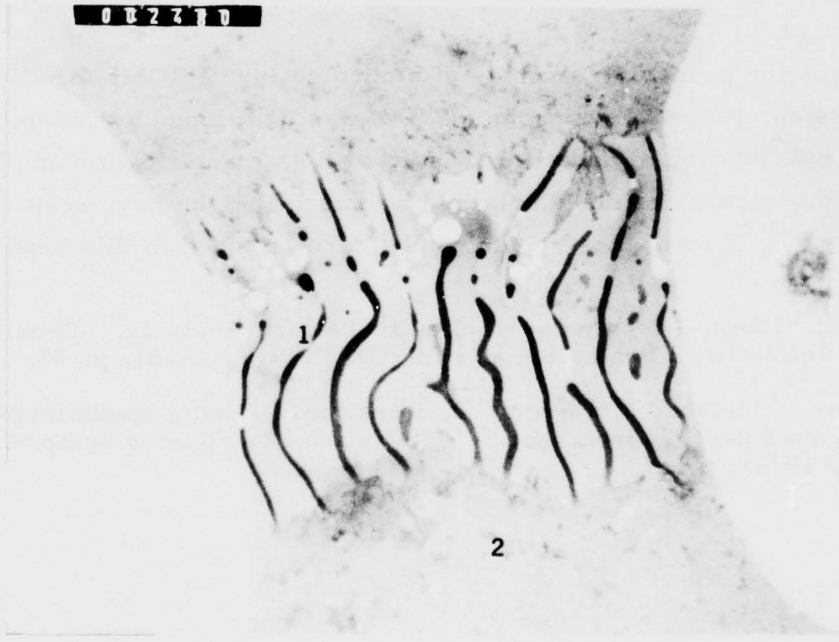

Figure 24. TEM photo of nichrome fuse gap, vendor A. (Width at middle ~ 3.1 μm.)

The other type of fuse link, as used by vendor B, is shown in Figure 25. Here the NiCr remaining in the gap is in the form of circular particles and short filaments. They are interconnected with a network of Ni-Cr spinel and with much greater gap void than for the first type of fuse.

The programming mechanism described by Kenney et al.[6, 7] is based on theories of disintegration of liquid sheets. The first step in programming is joule heating of the nichrome fuse to its melting point by the electric current passing through it. Next, one or more holes in the nichrome film, formed before or after melting by impurities in the film, metal migration under the influence of the electric current or field, or some other influence, grow larger due to the surface tension of the liquid metal. Perturbations then develop on the rim of the hole which cause it to break up into symmetrical filaments of nichrome. The filaments may also break up into particles (droplets) if the temperature and size of the fuse gap are suitable. The spacing

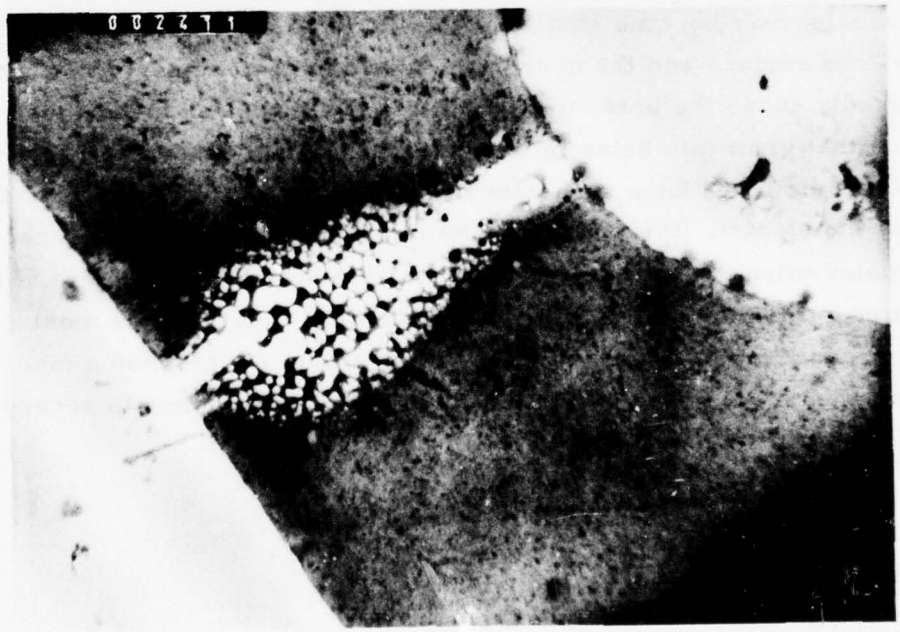

Figure 25. TEM photo of nichrome fuse gap, vendor B.
(Fuse width at gap ~3.8 μm)

of the nichrome filaments and particles can be calculated from the theories of Rayleigh and Weber; the results[6] are in rough agreement with the observations. As soon as a filament is broken, its source of heat (the electric current) is removed and it soon solidifies as a result of heat loss by conduction to the overlying passivation glass and the underlying oxide and silicon.

The spinel film observed in the gap where the nichrome has withdrawn is the oxide that formed on the surface of the nichrome. During programming, it becomes sufficiently hot in some spots to break up under surface tension just as does the nichrome film. Since the spinel probably melts at a higher temperature than the nichrome and is heated only by contact with nichrome (since its electrical conductivity is low), the degree of its breakup is less than it is for the nichrome.

The qualitative agreement between structural features predicted by the theories of the disintegration of liquid sheets and the observations of nichrome fuses by the SEM[9] and the TEM[6,7] is impressive. The calculated filament and droplet spacings do not agree closely with the observed values, perhaps because the values of surface tension, viscosity, and temperature required for the calculations are uncertain. However, the influence of the overlying passivation glass may also be important. During programming, it is heated and its viscosity may become small but the liquid nichrome film still will not have a free surface and the overglass should inhibit the perturbations that supposedly cause the breakup of the film. The mechanism for nucleation of the voids that grow into holes is uncertain, although it is conceivable that the thin nichrome films have sufficient imperfections which act as void nuclei. The role of the electric field acting on the liquid metal ions, as evidenced by the asymmetry often detected in the gaps, is also not clear. In spite of the uncertainties remaining, the liquid sheet instability theory is the most inclusive explanation of the programming mechanism for nichrome fuse memory elements. It is likely that it can be developed further to account for the uncertainties if necessary.

6. MEMORY ELEMENT FAILURE MECHANISMS

PROM element failures involve conversion of an unprogrammed element into a programmed element and vice versa. Information about failures has been obtained from two types of sources: life tests and user's field experiences. Under this program, life tests of programmed PROMs were conducted at elevated temperature for durations of more than 2000 hours (see Section 7). The results of tests conducted elsewhere have also been considered. User information was obtained from various Hughes program from the Reliability Analysis Center Report,[16] from published data, and from responses to a questionnaire sent out as part of this program. In addition to failures that have actually been observed, other possible failure mechanisms are described where appropriate, based on the detailed analyses of PROM devices which were made during this program. Failures of the input-output and addressing circuits also occur but are not considered here.

POLYSILICON FUSE FAILURE MECHANISMS

Unintentional conversion of an unprogrammed fuse link into a programmed fuse might be effected either by corrosion or by the read current. In the case of polysilicon fuse links, corrosion is not expected to be the threat that it is for NiCr fuse links. This is due to the much greater thickness of the polysilicon film and to the protective oxide that forms on Si. This was verified by performing the passivation integrity tests specified for NiCr fuse PROMs (see section on nichrome fuse failure mechamisms) on 1024-bit polysilicon fuse PROMs. Twelve unprogrammed parts and one programmed part were put through the freeze-out test (per MIL-M-38510/201, paragraph 4.3e) and no electrical changes were detected. Then two unprogrammed parts were opened for the water drop test (paragraph 4.4.2c of the same specification)

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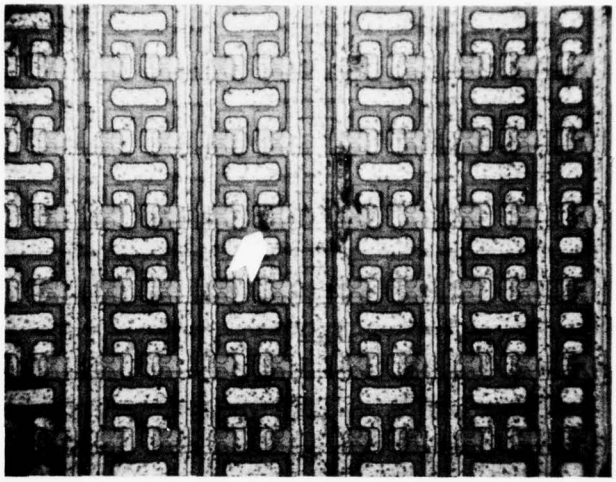
[16] H.C. Rickers, "Microcircuit Device Reliability: Memory/LSI Data," Reliability Analysis Center report MDR-3 (Rome Air Development Center, Winter 1975-1976).

by grinding off the lids and each was placed in a DIP socket wired so as to energize locations near the center of the chip (row 15, column 7 of each bit). With the devices energized, a droplet of high resistivity water was placed in the middle of the chip with a glass pipette. As each droplet evaporated, another was deposited so that the total time with water on each chip was at least three minutes, as directed in the specification. Afterwards, the devices were read out. Two addresses on one sample and one on the other had apparently become programmed.

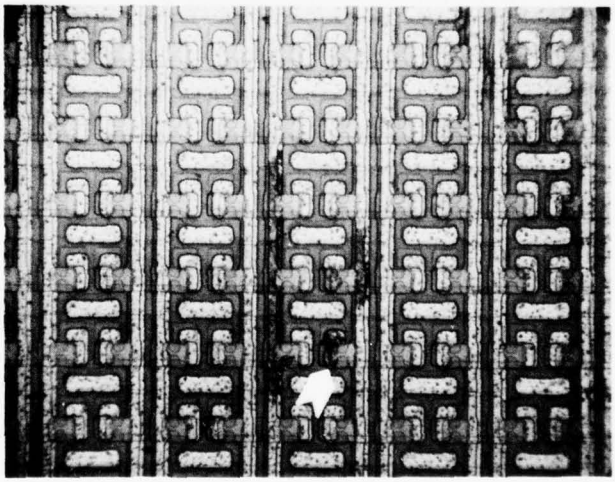
Microphotographs of portions of one of the two devices are shown in Figure 26. The two memory elements which became programmed are indicated. The polysilicon fuse links are intact but the Al lines that connect the fuses to the transistor emitter contacts are corroded. Some corrosion of Al column buses also occurred, apparently through cracks along the edges of the Al lines, but the polysilicon stripes underlying those buses provided sufficient conductivity to avoid further bit changes. (The fuse-emitter conductors do not have underlying polysilicon.) The same phenomenon occurred on the second water drop test sample. Since the overglass passivation is removed from the polysilicon fuse areas to facilitate programming, thereby exposing portions of the Al metallization, it is not surprising that some corrosion occurred on these devices. However, no corrosion of the polysilicon was observed anywhere, which confirms the expectation that failure by corrosion of the fuse link is not likely for polysilicon fuse PROMs.

The other possible mechanism for failure of an unprogrammed polysilicon fuse link is fusing by the read current. The power dissipated in the fuse link during read is only 0.625 mW, which is 0.7 percent of the normal programming power, so fusing during read will only occur for exceptionally narrow fuses. Tests by one manufacturer showed that this may occur for widths of 0.3 μm or less.[17] That manufacturer's data showed that the average fuse width is 2.2 μm and the chance of obtaining fuses narrower

[17] R. C. Smith, S. J. Rosenberg, and C. R. Barrett, "Reliability Studies of Polysilicon Fusible Link PROM's," Proc. IEEE 1976 Reliability Physics Symposium (IEEE, N.Y., 1976); Bill Pascoe, "Polysilicon Fuse Bipolar PROMs," Intel report RR-9 (Intel Corp, Santa Clara, CA, 1975).



a. Bit 0, row 16, column 3.



b. Bit 1, row 6, column 7.

Figure 26. Programmed locations as result of water drop test on polysilicon fuse PROM sample 12.

than 1 μm in normal production is only 0.01 percent. However, this dimension is not inspected so devices with such fuses could occur. No failures of unprogrammed polysilicon fuses were detected during this program and none have been reported from other sources.

The second failure mode for fuse link PROMs, reversion of a programmed link back into an apparently unprogrammed condition, is called reconduction. During normal programming, a physical gap is produced in a polysilicon fuse link. This gap contains some SiO_2 formed during fusing. This oxide and the native oxide formed on the surface of the polysilicon are probably adequate to prevent accidental reconduction by a loose metallic particle coming to rest on top of a blown fuse. However, the width of the gap in the polysilicon link can be very small, as shown in some of the transmission electron microscope photos in Section 5. The thin dielectric film in these narrow gaps may be prone to reconduction under certain voltage and temperature conditions. As described in the previous report by Hughes Aircraft Company,[9] reconduction may result from conductance through the dielectric at high temperatures or electrical breakdown. Since the melting point of Si is close to that of NiCr and melting may be involved in forming a permanent reconduction[9] (if such exists), the susceptibility of polysilicon fuses to reconduction might be similar to NiCr fuses. In both cases, however, most reconductions are probably unstable and are a result of incompletely programmed fuse links.

Reconduction of polysilicon fuse links on one part has been reported.[18] This occurred after dynamic burn-in on three bits of a 1024-bit device manufactured in early 1975. The reconducted fuse links had resistances of 500 to 900 ohms, less than the minimum resistance for a fuse to appear programmed (1000 ohm) but larger than the unprogrammed fuse resistance, 100 ohm (see Section 2). Examination with a scanning electron microscope showed that most of the programmed fuse links on that part had narrow gaps.

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[18] D. G. Platteter (Naval Weapons Support Center, Crane, Indiana), private communication (July 1975).

The photograph of one reconducted fuse (Figure 27) shows that it resembles fuses blown under reduced power during this program, such as the one shown in Figure 14d. Unfortunately, the programming parameters for the reconducted fuse are not known, but the manufacturer believes it was incorrectly programmed. Its superficial appearance suggests that a limitation on the number of pulses used to program polysilicon fuse PROMs could reduce the occurrence of this type of failure.

No other failures of polysilicon fuse elements have been reported. None were detected during the tests conducted as part of this program on those fuses programmed according to the manufacturer's recommendations.

AIM FAILURE MECHANISMS

No failures of unprogrammed AIM PROM elements have been reported by users contacted under the present study and none were obtained in the life test program (see Section 7) or in other programs.[8] One failure of a programmed AIM memory element was reported earlier[9] but its cause was not definitely determined. No other programmed AIM bit failures have been reported by users and none have been detected in accelerated life tests. Therefore only hypothetical failure mechanisms are discussed for this type of PROM element.

An unprogrammed AIM memory element would require an emitter-base short in order for it to appear as programmed. No contact is made to the bases of the memory element transistors and they are protected by SiO_2 and passivation glass. Shorting by loose particles on the surface of the chip is therefore unlikely. The read current is only 0.25 percent of the programming current so formation of a short by junction breakdown during normal use is also not likely.

Another possible failure mechanism for unprogrammed AIM elements is sufficient growth of alloying pits to short the emitter-base junction. These pits, which form as a result of diffusion of Si into the overlying Al metallization during the contact sintering step in normal processing,[12] appear to penetrate one third or more through the emitter region in some cases (see Figure 23).

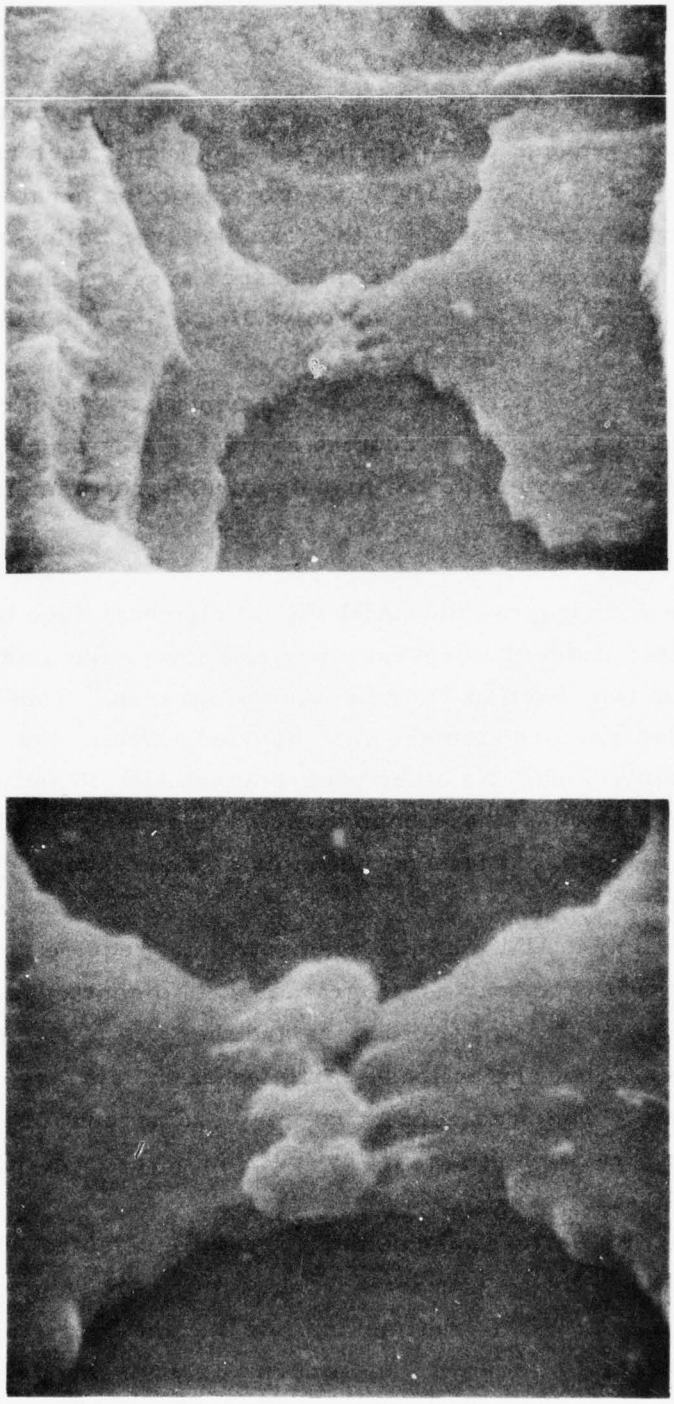

Figure 27. SEM photos of programmed polysilicon fuse link that reconducted after dynamic burn-in. (Fuse width at narrowest point ~2 μm.)

Short-circuiting of emitter-base junctions, presumably as a result of contact sintering, has occurred [10] with shallow transistors on (100) Si, which is the orientation used for AIM PROMs. At the high temperature limit for military integrated circuits, 125°C, the growth rate of alloying pits will be much less than the rate at the sintering temperature. This is caused by the exponential dependence of diffusion coefficient (D) on temperature:[19] $D=D_o \exp(-Q/kT)$, where D_o is a constant, Q is an activation energy, k is Boltzmann's constant, and T is the temperature (°K). Using Q = 0.79 eV for the diffusion of Si into thin film Al[12] and assuming that the Al fills the growing alloying pit by a diffusion process with a much lower (i.e., negligible) activation energy, the ratio of the diffusion coefficient at the sintering temperature (425°C) to that at the maximum use temperature (125°C) is 2×10^4.

The characteristic distance for diffusion[19] is proportional to $(Dt)^{1/2}$, where t is the time at a particular temperature. Assuming that the characteristic diffusion distance of Si in the overlying Al is proportional to the depth of the alloying pits, the time required for a pit to grow at 125°C from one third through the emitter region to the emitter-base junction can be estimated using the characteristic distance formula. This time will be the difference between the time required for a pit to grow all the way from the contact to the junction (distance = X) and the time required for it to grow one-third the distance (distance = X/3): $\Delta t \cong X^2/D(125^\circ) - (X/3)^2/D(125^\circ) = 8X^2/9D(125^\circ)$. From the pits produced during contact sintering, $X/3 \cong [D(425^\circ)\, t(425^\circ O)]^{1/2}$. Hence, $\Delta t \cong 8t(425^\circ)D(425^\circ)/D(125^\circ)$. Substituting the sintering time of 4m and the ratio diffusion coefficients given above, one obtains

$$\Delta t \cong (8)(4\ m)(2 \times 10^4) = 64 \times 10^4\ m$$

$$\cong 10,700\ h.$$

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[19] P. G. Shewmon, Diffusion in Solids (McGraw-Hill, N.Y., 1963).

Thus, the change of unprogrammed AIM PROM elements into programmed ones by the mechanism of alloying pit growth is estimated to occur after 10,000 hours at 125°C. However, no failure of this nature has been reported (see Section 7), even for exposures at 125°C for more than 10,000 hours.[8] The analysis presented here, which ignores the limited solubility of Si in Al, is simplified and is likely an underestimate of the time before failure. Therefore, this failure mechanism is probably not a serious threat to the reliability of AIM PROMs.

For programmed AIM memory elements, opening of the emitter-base conductive path would be required for them to revert to the unprogrammed condition. The penetration of the Al finger through the junction during programming (see Section 5) is not a reversible process and the read current is in the same direction as the programming current. Therefore opening of the conductive path is not likely to occur.

There may be a possibility of the Al finger penetrating further and shorting the base-collector junction as well as the emitter-base junction, thereby disabling an entire row of PROM elements. The small read current is insufficient to cause the local heating that is believed to be responsible for initiating programming, especially since the resistance of the programmed junction is less than ten ohms. However, Al will gradually diffuse from the finger into the surrounding Si. The diffusion coefficient for this process at the maximum operating temperature, 125°C, has not been determined[12] but it is probably much smaller than that for the diffusion of Si into Al, which was considered for the alloying pit case above. Since Al is a p-type impurity in Si, this diffusion may merely increase the local carrier concentration of the p-type base region and push the base-collector junction further into the collector region without affecting the operation of the device. Therefore, additional penetration of the Al finger during operation is not expected to be a failure mechanism of AIM PROMs.

Another possible failure mechanism is a short between the Al metal layer that makes contact with the emitters of the memory element transistors and the overlying Al bus for the collectors of the memory elements. The top surface of the Al on the emitter contacts of a partially programmed AIM PROM was revealed by etching away the overlying Al and glass films.

Under scanning electron microscope examination, no significant difference between the programmed and unprogrammed locations was detected. Therefore the risk of failure by this mechanism appears to be independent of programming and the same as for multilevel metallization in integrated circuits. One incident of "metallization short" was the only die-related malfunction reported for AIM PROMs by the Reliability Analysis Center.[16]

NICHROME FUSE FAILURE MECHANISMS

The failure modes of nichrome fuse links are the opening of an unprogrammed link and the reconduction of a programmed link. The failure mechanism for the first mode is corrosion of the nichrome through cracks or pinholes in the passivation glass; fusing by the read current has not been observed. The mechanism causing reconduction is still not clear. It may result from conductance through the dielectric (glass and spinel) at high temperature followed by electrical breakdown of the dielectric.[9] On the other hand, some of the observations made during the life tests indicate that reconduction of NiCr fuse links may be unstable and probably results from incompletely programmed links (see Section 7). The failure mechanisms for NiCr fuses were thoroughly discussed in the earlier report by Hughes[9] and references to many other discussions are given in the recent paper by Franklin.[20]

Fourteen die-related malfunctions of NiCr PROMs were recorded in the recent Reliability Analysis Center (RAC) report.[16] Half of these were on parts having gold-doped transistors, which were used on the parts from one vendor in the previous evaluation of PROMs by Hughes.[9] Less than four of these seven failures were related to a fuse link but at least one of them was a "growback" (reconduction) of a fuse on a 256-bit part. Another 14 reconduction failures under 125°C burn-in conditions were reported by users. Details of these failures are given in the Table on User Test Results, in Section 7.

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[20] P. Franklin, "A Reliability Assessment of Bipolar PROMs," Proc. IEEE 1976 Reliability Physics Symposium (IEEE, N.Y., 1976).

Schottky-clamped transistors are used in all of the NiCr fuse PROMs evaluated in this program and in the PROMs obtained from Vendor A for the previous evaluation.[9] None of the seven malfunctions reported by RAC for Schottky PROMs involved the NiCr fuse links. According to the PROM life data summarized in the RAC report,[16] the number of failures of all types per part-hour during static and dynamic tests at 125°C is similar for the two transistor technologies. There should be no reason to expect that the recent change from gold-doped to Schottky transistors (see Section 2) will affect the reliability of NiCr PROMs.

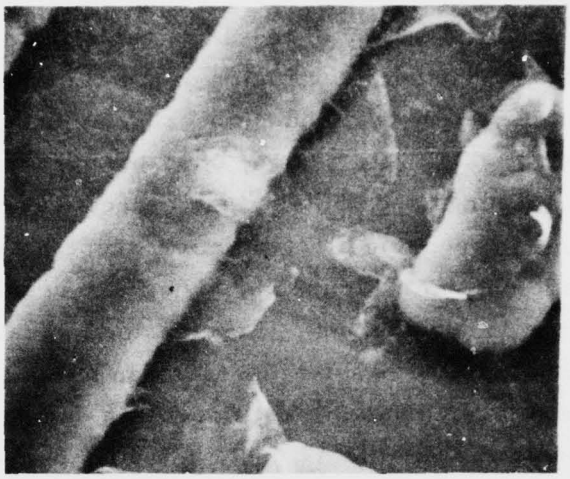
The mechanism of failure due to corrosion of NiCr is guarded against by coating the PROM with a passivation film of phosphosilicate glass (see Section 2). The adequacy of the overlay passivation was tested by the procedure in MIL-M-38510/201, which is a specification for 512-bit NiCr PROMs. Samples of 1024, 2048, and 4096-bit PROMs were tested, one of each size from Vendor A and two of each from Vendor B. The procedures used are listed below.

1. Electrical read-out to verify that device is unprogrammed.
2. Temperature cycling from -65°C to +150°C, per MIL-STD-883A, Method 1010.1, test condition C.
3. Freeze-out test, per MIL-M-38510/201, paragraph 4.3e.
4. Electrical read-out to see if any changes occurred.
5. Open package by grinding off the ceramic lid or by unsoldering the metal lid, as appropriate.
6. Water drop test, per MIL-M-38510/201, paragraph 4.4.2c.
7. Electrical read-out to see if any changes occurred.
8. Inspect with an optical microscope and perhaps with a scanning electron microscope to identify the nature of any changes that occurred.

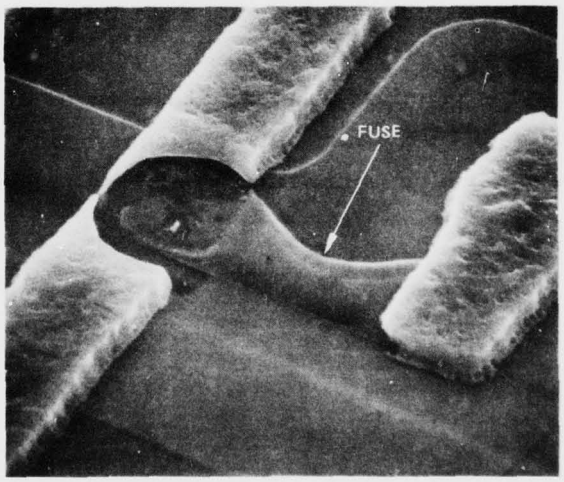
The purpose of the temperature cycling is to stress the device and produce cracks in the passivation glass if possible. The freeze-out test is intended to produce a film of water on the chip while power is applied, thereby producing electrocorrosion of metal lines through any pinholes or cracks in the passivation glass. The water drop test is a destructive test in which an attempt is made to produce electrocorrosion by applying high resistivity water directly onto the PROM chip while power is applied.

No electrical changes as a result of temperature cycling and the freeze-out test were detected on any of the samples. After the water drop tests, no changes occurred on any of the three parts from Vendor A. On one 2048-bit part from Vendor B, a portion of the aluminum V_{cc} bus was etched away without any electrical change because an underlying diffused conductor was in parallel with it. On one 4096-bit part from Vendor B, four multi-bit electrical failures and one single-bit electrical failure were caused by etching of Al lines. Scanning electron microscope photographs of the single-bit failure are shown in Figure 28. The flaky residues in 28a were left after the water drop evaporated. These photos indicate that the failure resulted from a pinhole in the passivation glass on top of the Al line where it contacted the end of a NiCr fuse link. Corrosion during the water drop test apparently dissolved away the Al under the pinhole and destroyed the Al-NiCr interface, judging from the partial corrosion of the underlying NiCr that is shown in Figure 28b. (The hole in the Al was enlarged by etching the part for two minutes in HCl before the passivation glass was removed.) No changes were observed in the other four parts from Vendor B.

The test results of the NiCr fuse overlay indicate that the passivation is adequate. No corrosion failures of the NiCr fuse links were observed either in these tests or in the life tests conducted during this program. No evidence of cracks was seen in the passivation glass at the edges of the Al metallization lines that contact the ends of the fuse links. Occasional pinholes were detected in the passivation layer, which is considered normal for integrated circuits.



a. Before etching.



b. After Al etch, followed by glass etch.

Figure 28. Aluminum metallization failure made during water drop test on nichrome fuse PROM. (Diagonal aluminum line width is ~4 μm.)

7. BURN-IN AND LIFE TESTS

LIFE TESTS AND GENERAL INFORMATION

A 2016-hour life test was performed on 99 parts, approximately 25 parts from each of the four vendors included in this study. The purpose of this test was threefold: first, to learn as much about the failure rate of these devices as the limited sample size would permit; second, to determine the effectiveness of the burn-in screen and third, to evaluate the effects of required time to program on the reliability of programmed memory element To accomplish this, the samples were programmed under varying conditions as will be described below. The number of pulses required for programming each bit was recorded. All bits were programmed for each device. The programming was verified, and the samples were entered into a dynamic life test chamber at 125°C. The samples were periodically removed from the test and the stored data re-verified at room temperature to monitor the approximate time at which failure occurred. After 2016 hours, the devices were removed from test and the failed devices were analyzed to determine the cause. All of the failures were found to be individual bit changes. Selected failed devices were further analyzed with findings reported below.

The programming was done on a specially constructed fixture which permitted adjustment of the programming parameters, in particular the programming pulse amplitude. Associated with the programmer was an automatic recording device which monitored the number of pulses required to program each bit and printed on paper tape a coded number reflecting the approximate number of pulses required along with the octal address of that bit. Figure 29 shows a sample of this tape and an explanation of the code. The code is scaled to allow pulse counts up to 65,536.

The bits were programmed in two groups. The first group was programmed in accordance with the vendor's specifications. (The exact programming conditions are shown in Appendix III.) These bits were used to determine the failure rate of a properly programmed device. The second group of bits was programmed with programming pulse amplitude deliberately reduced below the recommended level. The result was to increase the number of pulses required

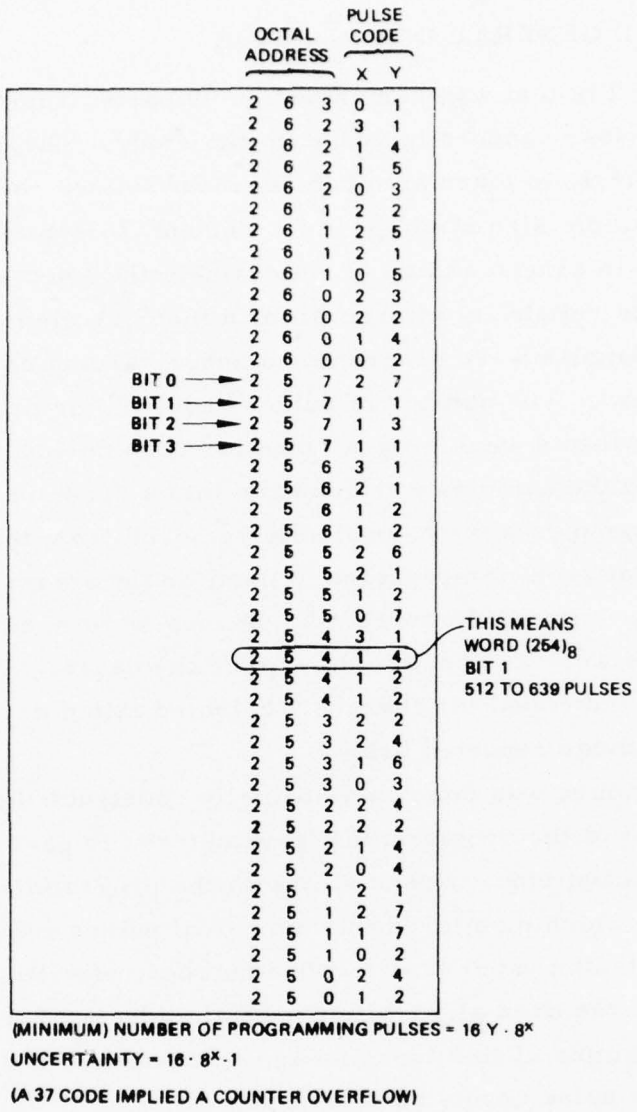


Figure 29. Sample of programming record tape.

for programming and the purpose of doing this was to deliberately induce marginal or failure prone memory elements, such as might result from the use of improper programming equipment. By noting the occurrence time of failures in the dynamic life test, the effectiveness of the burn-in screen could be evaluated.

After programming, the samples were inserted into burn-in sockets which provided the proper signals and biases for dynamic read operation. The V_{cc} bias was set at 5.5 V and the address inputs were cycled at a 1 MHz rate. The racks were placed in an oven at 125°C. The samples were removed from the oven and reverified after 24 hours and at increasing intervals over the 2016 hour test. Verification was done at room temperature and, in cases where the vendor recommended it, at reduced V_{cc} levels.

The results of the 2016 hour life test revealed no failures for the memory elements in the first group, which had been programmed according to the vendor's recommendations. The results of this portion of the tests are summarized in Table 9. As was expected, the second group produced a number of failures of the programmed fuses. The failure results for the second group are listed in Table 10. No failures were experienced in either group for the AIM devices. The same number of devices were life tested from each group. In general, half the bits from each group were programmed according to the vendor's specifications and the other half were programmed with long blow-times.

After completion of the life test, measurements were taken to further characterize the failures prior to delidding. It was found that increasing the V_{cc} bias to 5.5 V would correct several of the errors. Increasing the case temperature on devices from vendors A and B had a similar effect. Simultaneously raising the temperature and the V_{cc} bias would correct the majority of the errors. Conversely, lowering the temperature at reduced V_{cc} bias would cause new failures to appear.

Other anomalies were also observable. The number of errors observed at room temperature would sometimes change after a cycle of operation at high or low temperature. A high temperature cycle could result in a

TABLE 9. LIFE TEST SUMMARY WITH RESPECT TO PROGRAMMING WITH MANUFACTURER'S METHOD

Technology	Device Size (Bits)	Manufacturer	No. of Parts Life Tested	*Total No. of Bits Programmed with Manufacturer's Method	Total Life Test Part Hours	*Total Life Test Bit Hours x 10^6	Number of Failures
Polysilicon	1K	X	10	6144	20160	12.4	0
	2K	X	10	5120	20160	10.3	0
	4K	X	5	10240	10080	20.6	0
AIM	1K	Y	10	3072	20160	6.2	0
	2K	Y	10	5120	20160	10.3	0
	4K	Y	4	8191	8064	16.5	0
Nichrome	1K	A	10	2560	20160	5.2	0
		B	11	6044	22176	12.2	0
	2K	A	9	5120	18144	10.3	0
		B	10	10240	10240	20.6	0
	4K	A	5	10240	10080	20.6	0
		B	5	10240	10080	20.6	0
		Total	99	82331	189664	165.3	0

*Not including bits programmed with long blow-times.

TABLE 10. RECONDUCTION FAILURES OF FUSES PROGRAMMED WITH LONG BLOW-TIMES

Technology	Device Capacity (Bits)	Mfg.	No. of Fuse Failures at various hours of 125°C Life Test					
			24 hr.	168 hr.	336 hr.	672 hr.	1344 hr.	2016 hr.
Nichrome	1K	A	1	8	11	10	12	17
		B	1	4	7	8	5	6
	2K	A	0	1	3	1	3	4
		B	0	0	1	1	1	1
	4K	B	1	4	4	8	8	7
Polysilicon	2K	X	0	3	3	1	3	3
Total			3	20	29	29	32	38

reduced room temperature error count, and in a very few cases, a low temperature cycle would produce new errors at room temperature. Several months after the completion of the life test, the devices were again error checked. Still further changes in the error count were observed.

The unstable character of the some of the failed bits, as evidenced by these measurements, suggests that for many fuses a marginal failure condition exists as opposed to a solid data reversal. In this condition, even a slight change in the internal parameters caused by variation of temperature or voltage bias or by the progress of some physical process could result in a reversal of the output state. If the difficulties were caused by malfunction of the addressing or sensing circuitry, it is expected that the errors would lie in an orderly pattern, i.e., within a certain row, column, or bit. Since the location of the errors was more or less random, it appeared that the problem lies in the fuse elements themselves.

One sample from each of three vendors using fusible links was delidded and probed to determine the resistance of the fuses at the failed address locations. Table 11 gives the results of the measurements. The probing operation is rather difficult on these devices because of the minute size of the metallization areas. It was necessary to force the probe through the overglass to make electrical contact, as it was felt that chemically stripping the glass would modify the fuse resistance and obscure the results. Even so, it is possible that the delidding and probing operations could have affected a tenuously conducting fuse. Even though the data is not entirely consistent, it does present evidence that the failures were caused by fuses whose resistances were very low compared to that of a properly programmed fuse. The fuses that measured in the Megohm region are not readily explainable. It can only be speculated that the fuses were probably disturbed and the low resistance connections reopened.

TABLE 11. RESISTANCE MEASUREMENTS ON FAILED FUSE ELEMENTS

Vendor X (Polysilicon)	Vendor B (Nichrome)	Vendor A (Nichrome)
200Ω	>1 megΩ	2500Ω
150Ω	>1 megΩ	2100Ω
900Ω	>1 megΩ	2500Ω
150Ω	>1 megΩ	2400Ω
300Ω	>1 megΩ	2100Ω
100Ω	840Ω	3000Ω
600Ω	2000Ω	1900Ω
	>1 megΩ	2000Ω
	>1 megΩ	2500Ω
		2100Ω

The samples showing temperature dependent errors provided an opportunity to check another aspect of device behavior. Vendors A and B for nichrome PROMs recommend that after programming, verification should be carried out at reduced V_{cc} bias levels. Since this verification is generally performed at room temperature, it is important to know how effectively this test screens for marginal fuses over the full temperature range and normal V_{cc} tolerances. Using devices from Vendors A and B in which marginal fuses had been deliberately programmed as described above, the critical V_{cc} level at which the output data reversal occurred was measured. This measurement was repeated at -55°C, 25°C, and 125°C. The results are plotted in Figure 30 for two fuses which fail near the 4.5 V level at -55°C. A polysilicon fuse device was measured but only minor temperature effects were noted.

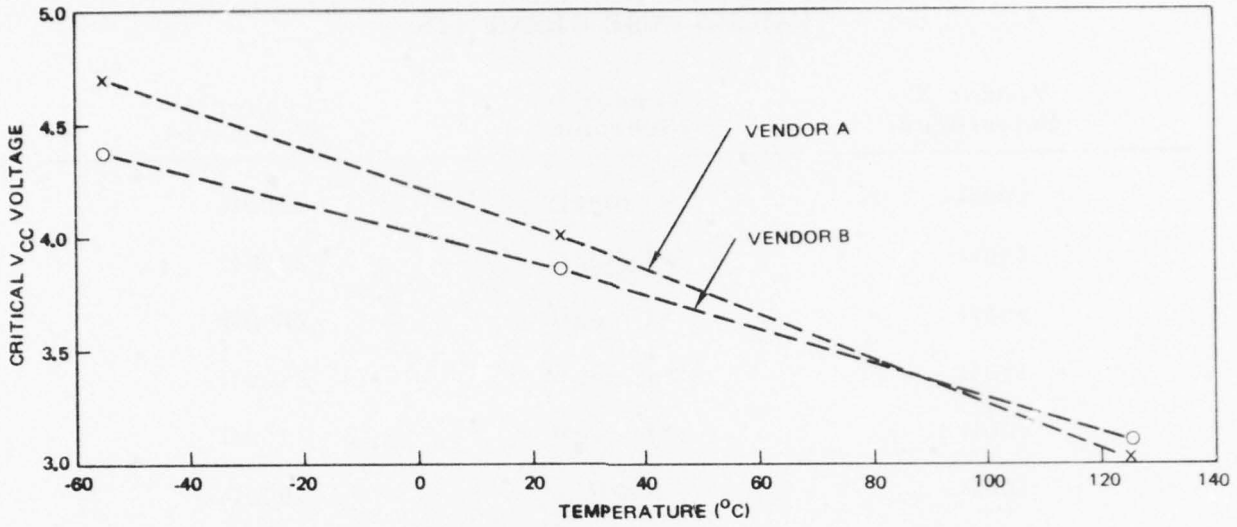


Figure 30. Critical V_{cc} bias versus temperature for marginal nichrome fuses (critical V_{cc} = bit reversal point).

Using these data, the critical V_{cc} level at 25°C could be estimated which would correspond to a failure at exactly 4.5 V at -55°C. The values obtained were 3.83 V for Vendor A and 3.96 V for Vendor B. These are somewhat below the upper limit of the minimum V_{cc} range allowed by the vendor's recommendations. It should also be noted that the above estimated values contain no safety margins to allow for drift in the fuse resistance or sense circuit parameters over the life of the devices.

Thus, if a reduced V_{cc} test is used as a substitute for full range temperature testing after programming, it would be necessary to further reduce the test level of the V_{cc} bias. This introduces the danger of rejecting good devices, since other parts of the circuitry may show malfunctions at very low levels of V_{cc} which do not correlate to a low temperature failure. Perhaps a second screening of the failed devices, at V_{cc} = 4.5 V and -55°C, would be cost effective in saving the good devices.

The verification should not be performed immediately after programming while the device is still at the elevated temperature caused by the high programming currents. This would lead to falsely optimistic results.

A separate life test was run to evaluate the stability of the programmed storage elements in the AIM devices. In these devices the resistance of a programmed element can be measured indirectly by deselecting the chip, addressing the desired word, and injecting 20 ma into the appropriate output terminal. This technique is used for verification during the programming operation. The resulting voltage measured at the same output terminal is an indirect measure of that across the storage element, but differs by the voltage drop across a base-emitter junction and two saturated transistors that lie in series along the current path. The pass-fail level this voltage during programming verification is approximately 7.0 V.

In the stability test, several locations on one device were programmed for varying lengths of time so that the voltages measured as described above ranged from 5.1 to 8.0 V. The device was then entered into dynamic life for 1147 hours, during which time the voltage was periodically monitored. The results of the measurements are shown in Table 12.

The resistance of the programmed devices seems to be very stable. The variations ranged from 1.2 to 21 percent. The location that was initially programmed to the 8.0 V level showed the greatest fluctuation. However, elements showing a verification voltage above 7.0 V would not occur in a correctly programmed device.

In addition to the tests described above, a survey of the testing experience of other users was made as described in Section 4 of this report. The results are summarized in Table 13. Based on the user data, the field experience appeared very good. In addition to other failures a number of reconduction failures occurred in 125°C burn-in tests.

TABLE 12. VOLTAGE MEASUREMENTS FOR STUDY OF STABILITY OF RESISTANCES OF PROGRAMMED AIM MEMORY ELEMENTS

	Measured Output Pin Voltage (20 mA Interrogation Current)				
Location	Initial	168 hours	336 hours	595 hours	1147 hours
1	7.2	7.2	7.3	7.8	7.3
2	6.5	6.7	6.6	6.9	6.5
3	6.8	7.5	7.7	7.7	7.9
4	7.1	7.0	6.9	6.9	6.9
5	7.1	7.0	7.0	7.1	7.1
6	7.5	7.0	7.0	7.0	7.0
7	8.0	7.8	8.0	6.3	7.7
8	5.6	5.6	5.7	5.7	5.7
9	5.3	5.6	5.6	5.7	5.6
10	5.1	5.6	5.6	5.6	5.6
11	5.4	5.7	5.7	5.6	5.7

AD-A048 231 HUGHES AIRCRAFT CO CULVER CITY CA STRATEGIC SYSTEMS DIV F/G 9/2
RELIABILITY EVALUATION OF PROGRAMMABLE READ-ONLY MEMORIES (PROM--ETC(U)
SEP 77 K L WONG, W W POWELL, R L LONG F30602-75-C-0294
UNCLASSIFIED HAC-P77-157R-PT-2 RADC-TR-77-302-PT-2 NL

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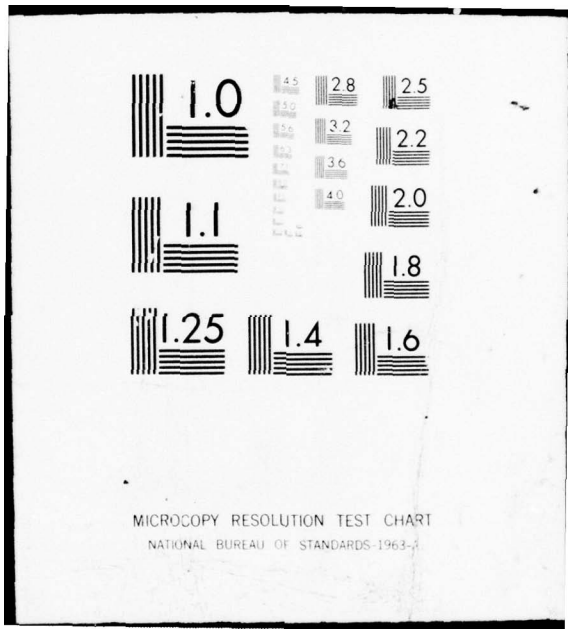
1.0
1.1
1.25
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1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
5.6
6.3
7.1
8.0
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

TABLE 13. USER TEST RESULTS

Technology	Device Size (Bits)	Manu-facturer*	Quality Level	No. of Parts Tested	Test	Number of Failures
Polysilicon	1K	X	Commercial	10	125°C 168 hours	3 - fuses measured 500 to 900 ohms on one part
	2K	X	Commercial	27	125°C 700 hours	0
Nichrome	1K	D	38510-B Equivalent	41	175°C 72 hours	3 - functional at 25, -55 & 125°C 4 - intermittent at -55°C 3 - functional at -55°C but passed with VIH increased by 10%
	2K	A	Commercial	29	125°C 700 hours	0
		B	Commercial	30	125°C 700 hours	1 - bit line leakage at 65 hrs. 1 - reconduction at 537 hrs.
		B	Commercial	22	125°C 4 day burn-in	1 - bit line leakage 1 - reconduction (20 burned-in parts used in field without failures)
		B	38510-B Equivalent	117	125°C 4 day burn-in	6 - bit line leakage 2 - word line leakage 12 - reconduction (80 burned-in parts used in field without failures)
Polysilicon Nichrome Titanium-Tungsten AIM	1K	Many	Commercial	900,000	Commercial equipment in field	Replacement rate is approximately 50 parts per month.

*D = Fairchild, see page 5 for other codes.

BURN-IN ANALYSIS

For a test designed to study the effects of burn-in, it is necessary that some failures occur during the burn-in period of the test. For the number of devices and memory elements available for this study, the quantity is not sufficient for accumulating any burn-in failures if the memory elements were programmed with the manufacturer's recommended methods. It was the consensus of the industry that the fuse reconduction problem is brought on by marginally blown fuses due to low current reaching the fuses. Therefore, for this study an effort was made to produce marginal fuses or AIM elements by means of lower than standard voltage pulses and the associated longer blow-times. No failure of any AIM device was experienced. However, for the fuses so blown with longer blow-times, there were many reconduction failures from the 125°C 2016 hours life test.

The numbers of device failures due to bit changes are tabulated in Table 14. The device is considered failed if it has one or more bit changes. The absolute numbers of failures with respect to the device types are not meaningful because the number of devices used and the number of bits programmed with long blow-times vary from type to type. However, the relative

TABLE 14. DEVICE BIT CHANGE FAILURES OF DEVICES PROGRAMMED WITH LONG BLOW-TIMES

Technology	Device Capacity (Bits)	Mfg.	Cumulative No. of Device Failures at various hours of 125°C Life Test					
			24 hr.	168 hr.	336 hr.	672 hr.	1344 hr.	2016 hr.
Nichrome	1K	A	1	5	6	6	6	6
		B	1	3	3	3	3	3
	2K	A	0	1	3	3	3	4
		B	0	0	1	1	1	1
	4K	B	1	2	3	3	3	3
Polysilicon	2K	X	0	2	2	2	2	2
Total			3	13	18	18	18	19

values with respect to test time within a device type or for the composite total are of interest. Table 15 gives percentages of cumulative failures with respect to the total number of failures at the end of the 125°C life test. Except for the 2K devices, which behave differently (as shown in Table 15), most of the failed devices occurred within 168 hours of test. The composite total showed that 68 percent of the failures occurred within 168 hours of test. A curve for the cumulative composite number of failures is plotted in Figure 31. This curve shows a distinct knee around 200 hours. By noting the occurrence of new device failures and the elpased time in each interval, a relative failure rate can be calculated for each interval. These relative failure rates are plotted in Figure 32. In the relative failure rate curve a knee appears around 300 hours. It indicates that after 300 hours, the occurrence of device failures settles down to a low and almost constant failure rate. This low failure rate is about 1/20 of the failure rate of the first day of life test. From a "total number of failures" view point, by 200 hours of operation a large percentage of the device failures would have occurred and further burn-in would be less efficient for screening out additional failures. However, from a failure rate standpoint, 300 hours would have been a better stopping point as the failure rate decreases to a low level without much change after this point. The exact burn-in time to be selected will therefore depend on the criterion one wishes to use, e.g., 200 hours for cost effectiveness and 300 hours for high reliability achievement. From a practical view

TABLE 15. PERCENTAGE CUMULATIVE DEVICE BIT CHANGE FAILURES OF DEVICES PROGRAMMED WITH LONG BLOW-TIMES

Technology	Device Capacity	Percentage of Cumulative No. of Device Failures at various hours of 125° Life Test					
		24 hr.	168 hr.	336 hr.	672 hr.	1344 hr.	2016 hr.
Nichrome	1K	22	89	100	100	100	100
	2K	0	20	75	75	75	100
	4K	33	66	100	100	100	100
Polysilicon	2K	0	100	100	100	100	100
Total		16	68	95	95	95	100

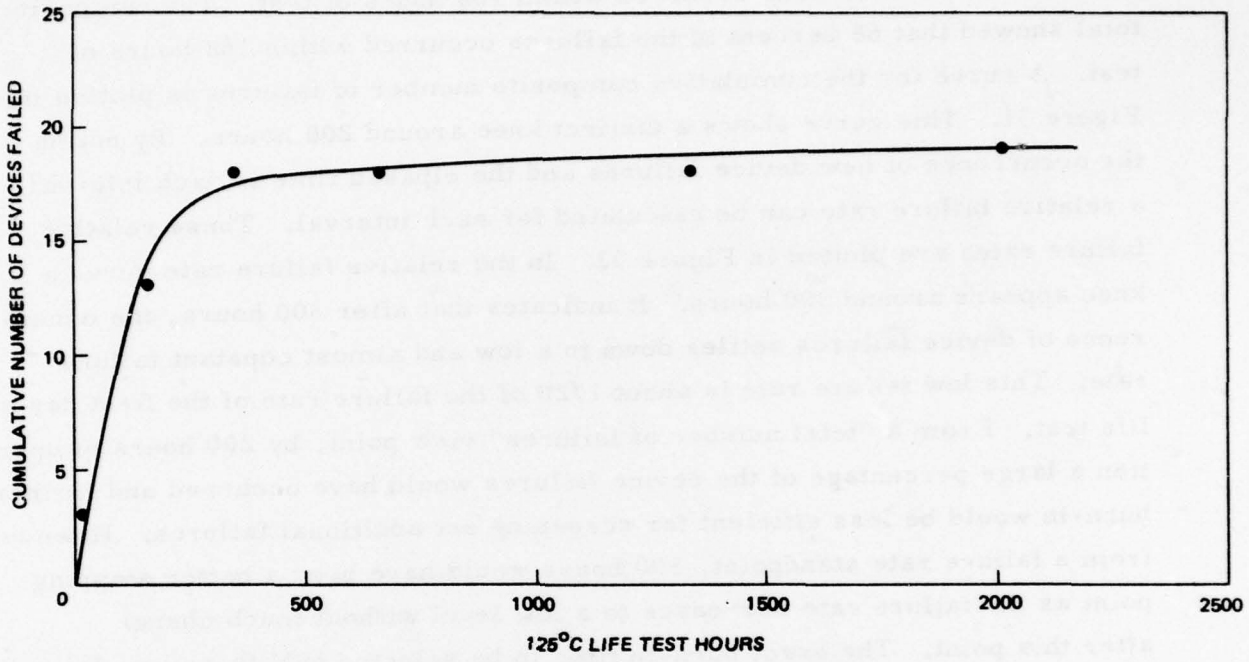

Figure 31. Composite cumulative number of fuse link devices failed because of bit changes as a function of life test time. (Devices were programmed with long blow-times.)

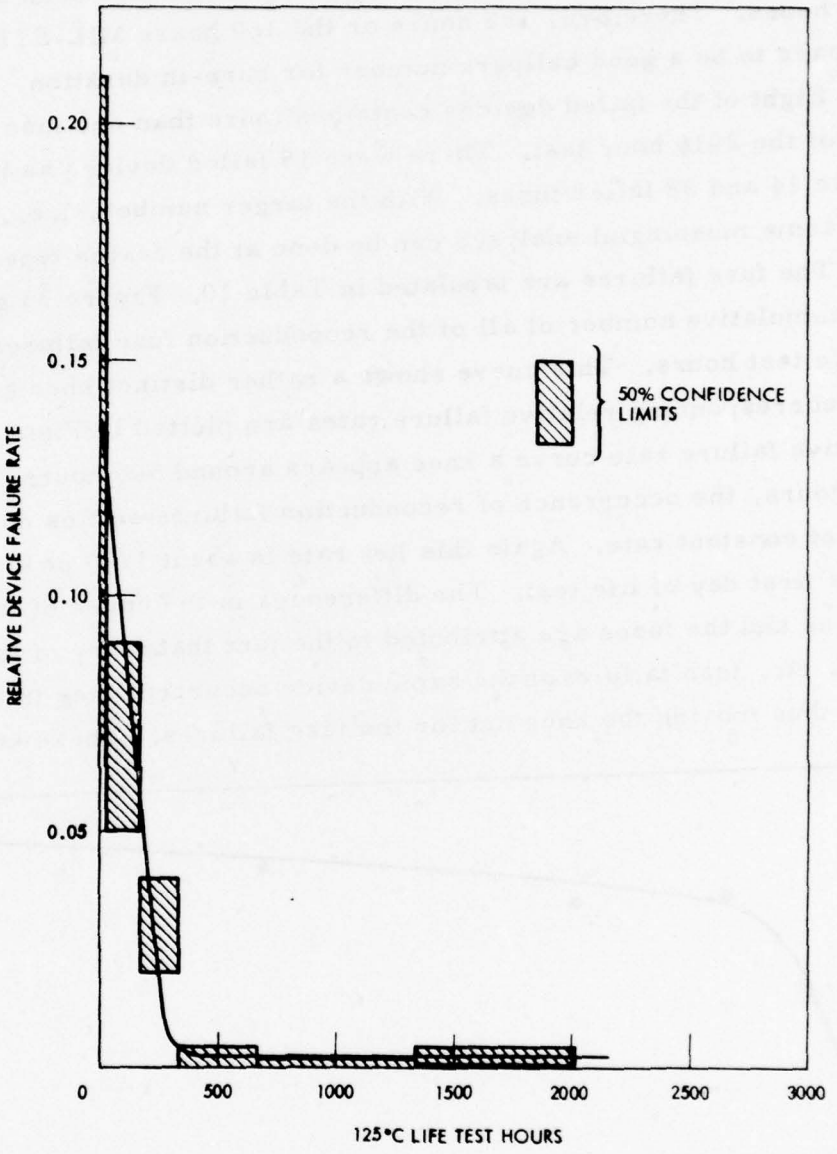

Figure 32. Composite relative failure rate of fuse link devices failed because of bit changes. (Devices were programmed with long blow-times.)

point the standard burn-time of 168 hours is very close to the knee and as indicated before 68 percent of the failures would have been screened out at 168 hours. Therefore, 168 hours or the 160 hours MIL-STD-883 figure appears to be a good ballpark number for burn-in duration.

Eight of the failed devices contained more than one fuse failure by the end of the 2016 hour test. There were 19 failed devices as indicated in Table 14 and 38 failed fuses. With the larger number, i.e., 38 instead of 19, some meaningful analyses can be done at the device type level.

The fuse failures are tabulated in Table 10. Figure 33 gives a plot of the cumulative number of all of the reconduction fuse failures as a function of life test hours. This curve shows a rather distinct knee around 250 hours. The corresponding relative failure rates are plotted in Figure 34. In the relative failure rate curve a knee appears around 500 hours. Thus, after 500 hours, the occurrence of reconduction failures settles down to a low and almost constant rate. Again this low rate is about 1/20 of the failure rate of the first day of life test. The differences in the knees of the curves for the devices and the fuses are attributed to the fact that many of the second, third, etc. fuse failures on the same device occurred later in time during the test, thus moving the knee out for the fuse failures. These knees of the

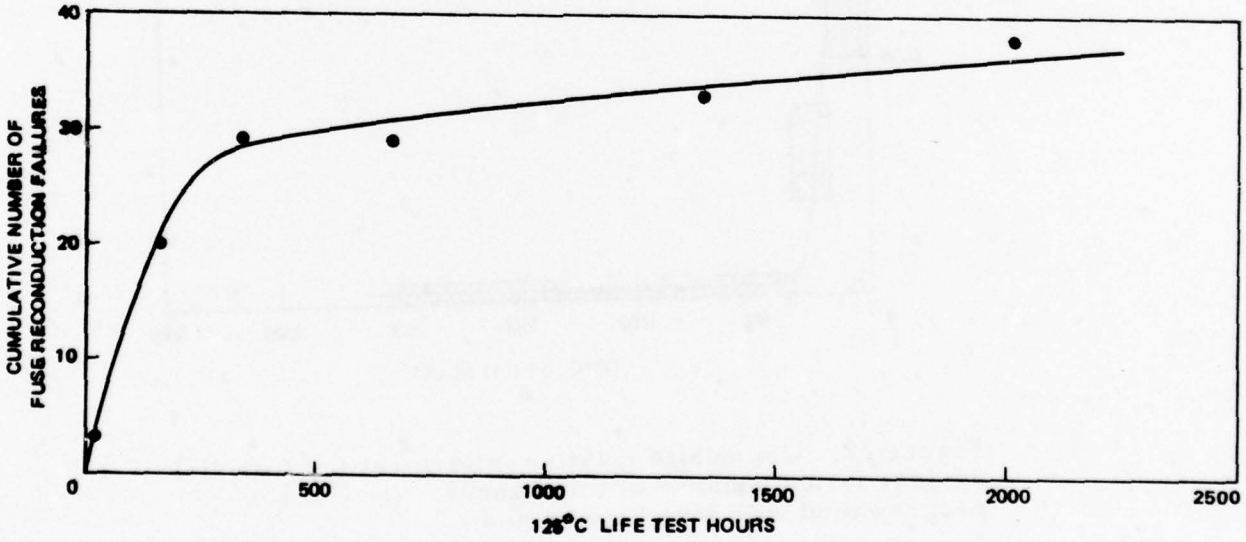

Figure 33. Composite cumulative number of fuse reconduction failures of NiCr and Si PROMs specially programmed with long blow-times as a function of life test time.

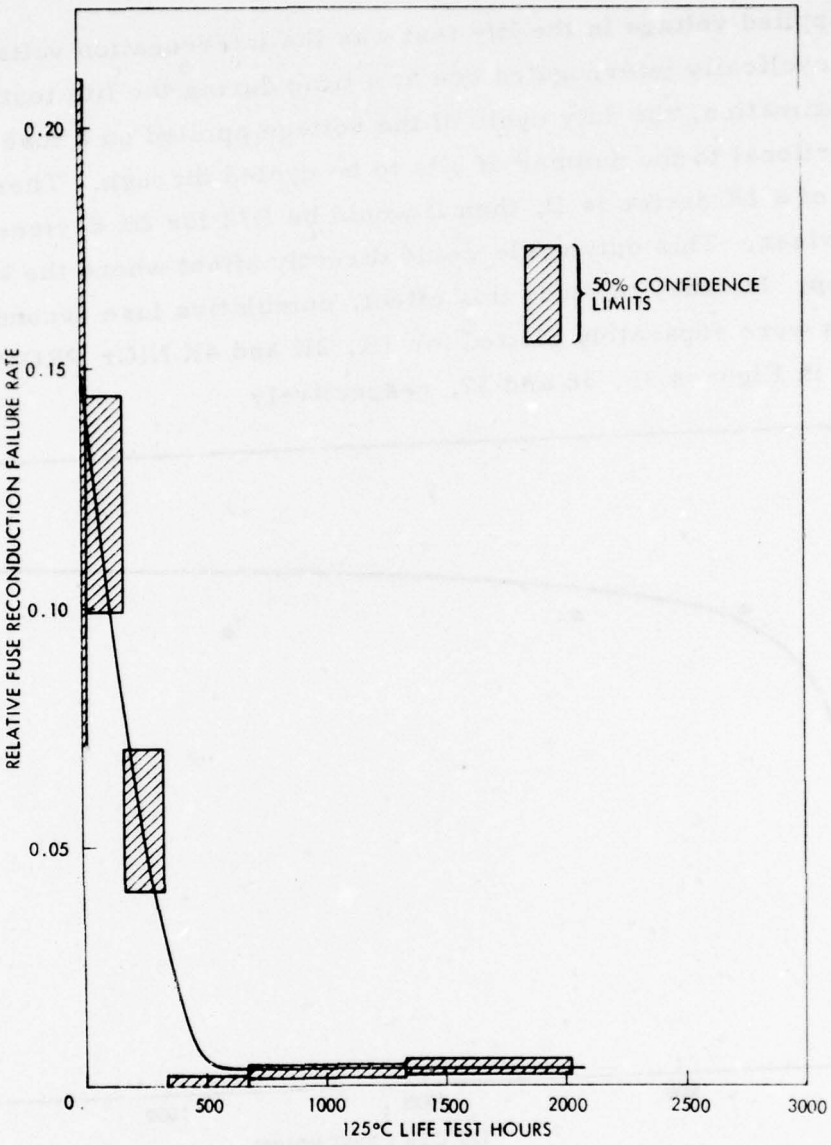

Figure 34. Composite relative fuse reconduction failure rate of NiCr and Si fuses specially programmed with long blow-times as a function of life test time.

curves are dependent upon how the life test is conducted. The life test condition needs to be examined further.

The report "Reliability Evaluation of Programmable Read-Only Memories"[2] postulated that fuse reconduction is akin to the breakdown of dielectric thin film and that the elapsed time between application of voltage to actual breakdown varies inversely as the applied voltage and temperature.

The applied voltage in the life test was the interrogation voltage. The bits were cyclically interrogated one at a time during the life test. As a first approximation, the duty cycle of the voltage applied on a fuse is inversely proportional to the number of bits to be cycled through. Therefore, if the duty cycle of a 1K device is D, then it would be D/2 for 2K devices and D/4 for 4K devices. This duty cycle would directly affect where the knee would develop. In order to study this effect, cumulative fuse reconduction failure curves were separately plotted for 1K, 2K and 4K NiCr PROMs and are shown in Figures 35, 36 and 37, respectively.

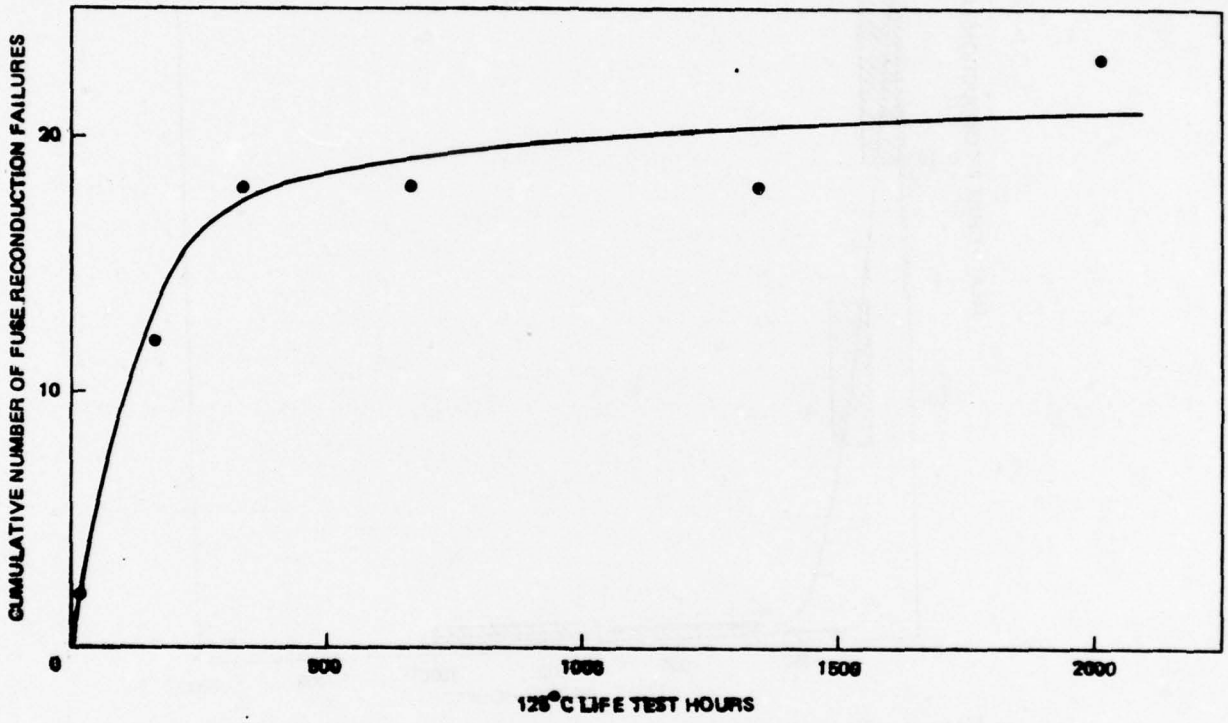

Figure 35. Cumulative number of fuse reconduction failures of 1K NiCr PROMs specially programmed with long blow-times as a function of life test time.

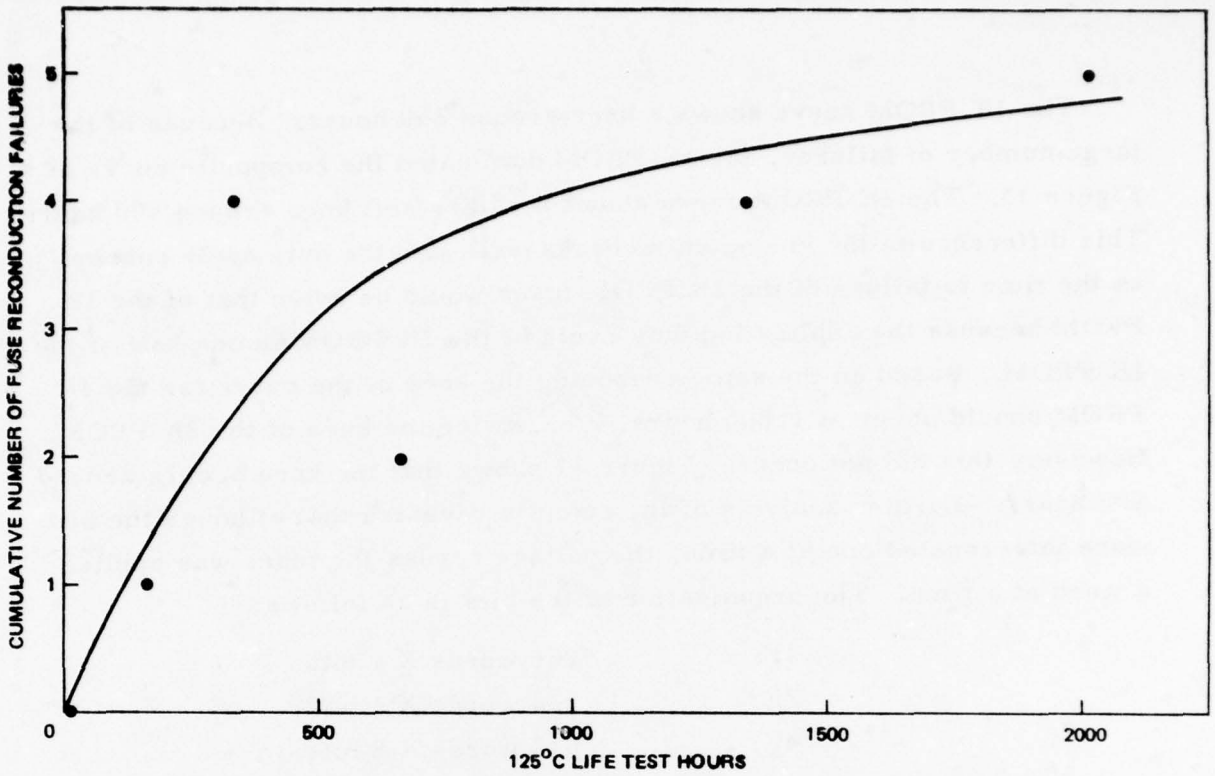

Figure 36. Cumulative number of fuse reconduction failures of 2K NiCr PROMs specially programmed with long blow-times as a function of life test time.

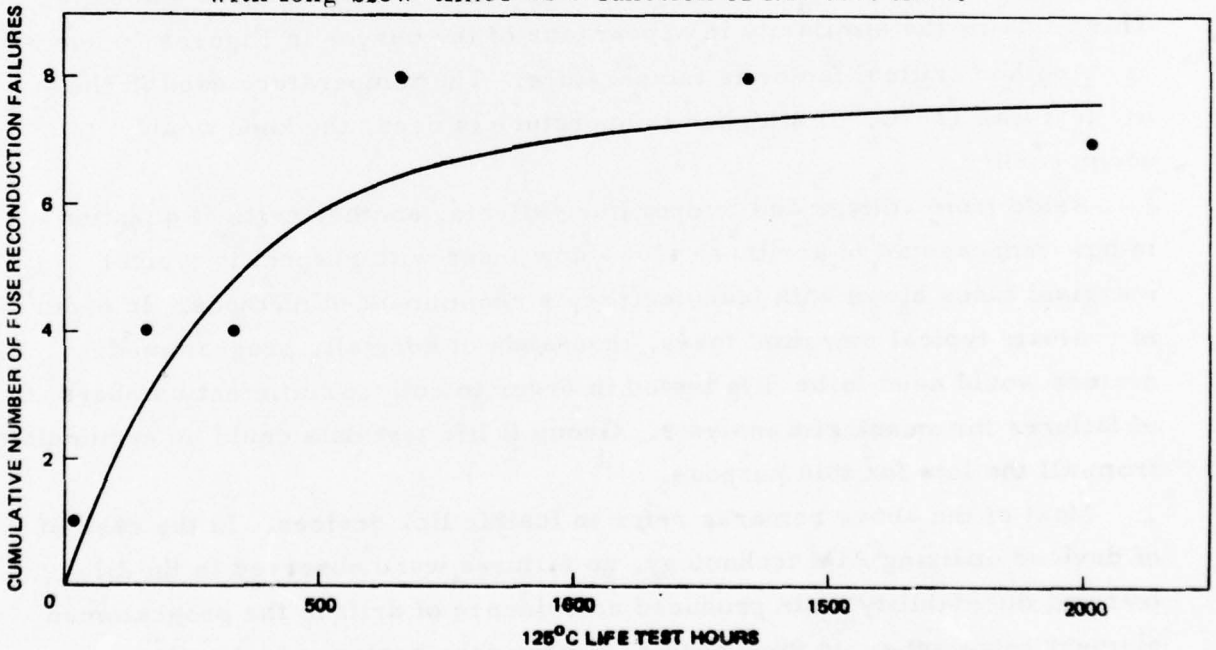

Figure 37. Cumulative number of fuse reconduction failures of 4K NiCr PROMs specially programmed with long blow-times as a function of life test time.

The 1K PROM curve shows a knee around 250 hours. Because of the large number of failures, the 1K PROM dominated the composite curve of Figure 33. The 2K PROM curve shows a rather soft knee around 500 hours. This difference in the knee points checks well with the duty cycle concept as the time to failure of the 2K PROM fuses would be twice that of the 1K PROM because the application duty cycle of the 2K PROM is one half of the 1K PROM. Based on the same reasoning the knee of the curve for the 4K PROM should occur at 1,000 hours, i.e., twice the knee of the 2K PROM. However, this did not occur. Figure 37 shows that the knee occurs around 500 hours. Further analysis of the circuits revealed that although the bits were interrogated one at a time, the voltage across the fuses was applied a word at a time. The organization of the bits is as follows:

1K:	256 words X 4 bits
2K:	512 words X 4 bits
4K:	512 words X 8 bits

Since the 2K PROMs and the 4K PROMs have the same number of words, the duty cycle of the voltage applied across the fuses will also be the same. This explains the similarity in appearance of the curves in Figures 36 and 37.

Another critical factor is temperature. The temperature used in the life test was 125°C. If a higher temperature is used, the knee would occur earlier.

Aside from voltage and temperature effects, another critical question is how representative are these slow-blow fuses with respect to typical marginal fuses blown with manufacturer's recommended methods. In order to evaluate typical marginal fuses, thousands of normally programmed devices would need to be life tested in order to collect sufficient numbers of failures for meaningful analysis. Group B life test data could be accumulated from all the lots for this purpose.

Most of the above remarks refer to fusible link devices. In the case of of devices utilizing AIM technology, no failures were observed in the life test and the stability tests produced no evidence of drift in the programmed element resistance. In view of this, perhaps the best conclusion that can be drawn is that the memory elements of the AIM devices do not contribute

appreciably to the failure rate and in regard to burn-in, these devices should be treated as any other semiconductor device of similar complexity.

PROGRAMMING TIME EFFECTS ON RELIABILITY

By use of lower programming pulse voltages, marginally programmed fuses were produced. After the 125°C, 2016 hours life test many reconduction failures occurred in these fuses. An attempt will be made here to correlate the failure rate with the time required to blow the fuses. As was discussed in the programming section the fuses were blown with a sequence of pulses instead of one long current pulse. For convenience of presentation, the number of pulses required to program will be considered instead of blow-times.

Table 16 is a tabulation of fuse reconduction failures and number of bits programmed in each category of pulses required to program the bits. It should be kept in mind that the pulse durations, voltages and shapes are different for the different vendors as described in Table 3. However, for the same vendors the programming conditions are essentially the same for devices of different bit capacities. The AIM devices, which did not have any failures, have been included in Table 16 to show that although long blow-times were also used on the AIM PROMs, apparently no marginal memory elements were created for these devices. This was confirmed by the identical appearances of the aluminum lumps at the emitter contacts for both the normally blown AIM junctions and the junctions blown with lower current pulses as discussed in the section on programming mechanisms.

In Table 16 it is observed that for vendor B nichrome 1K and 4K devices and vendor A nichrome 1K devices sufficient numbers of failures had occurred to enable calculation of failure rates and plotting of failure rate curves. The failure rate F is calculated by:

$$F = \frac{B}{NT} \text{ (failures per bit per hour)}$$

where B = Number of bit reversal failures

N = Number of bits programmed

T = Test time in hours, i.e. 2016 hours for the life test conducted.

Confidence limits on the number of bit reversals were first determined prior to the failure rate calculations. The resultant failure rate plots are shown in Figures 38 through 41. All of these plots show an increasing failure rate for the fuses blown with higher number of pulses. It is important that no reconduction failures were experienced for the 40,449 nichrome fuses programmed with less than 10 pulses. It should be noted that two vendors are included in the composite curve of Figure 41. The programming pulse

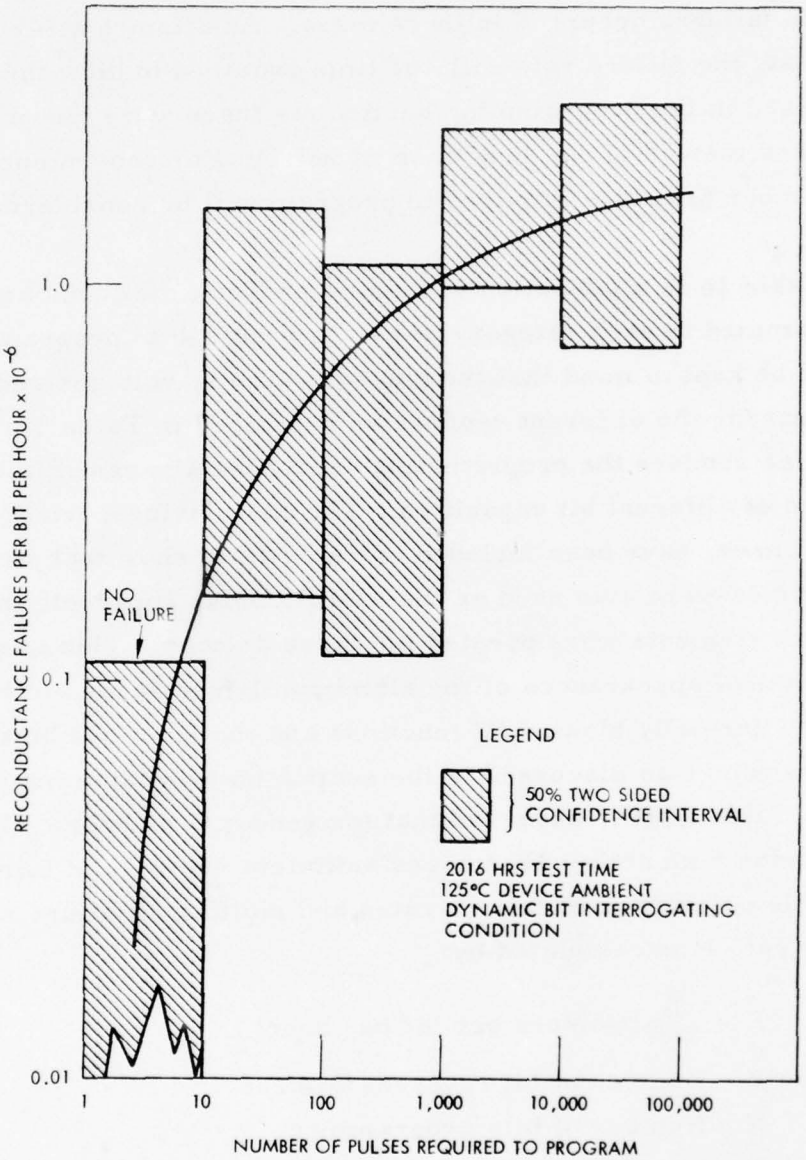

Figure 38. Reconductance failure rate versus number of pulses required to program for nichrome vendor B 1K devices. (Reduced voltage used in programming.)

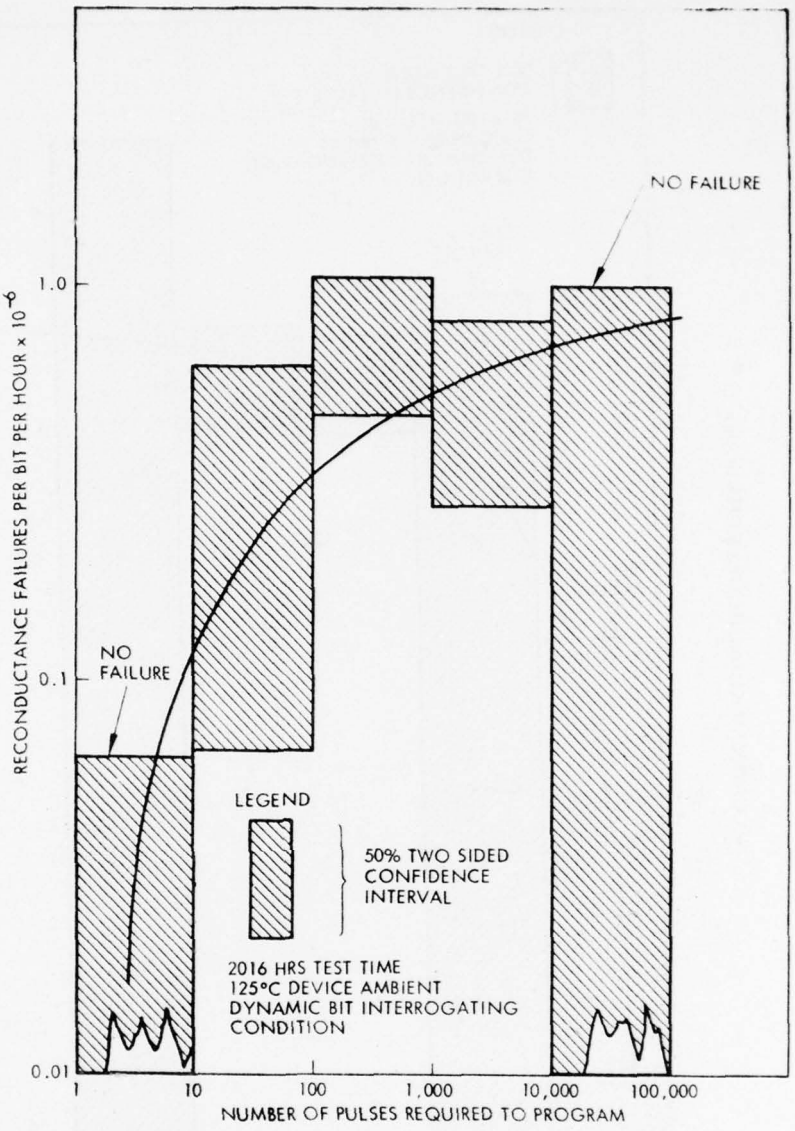

Figure 39. Reconductance failure rate versus number of pulses required to program for nichrome Vendor B 4K devices. (Reduced voltage used in programming.)

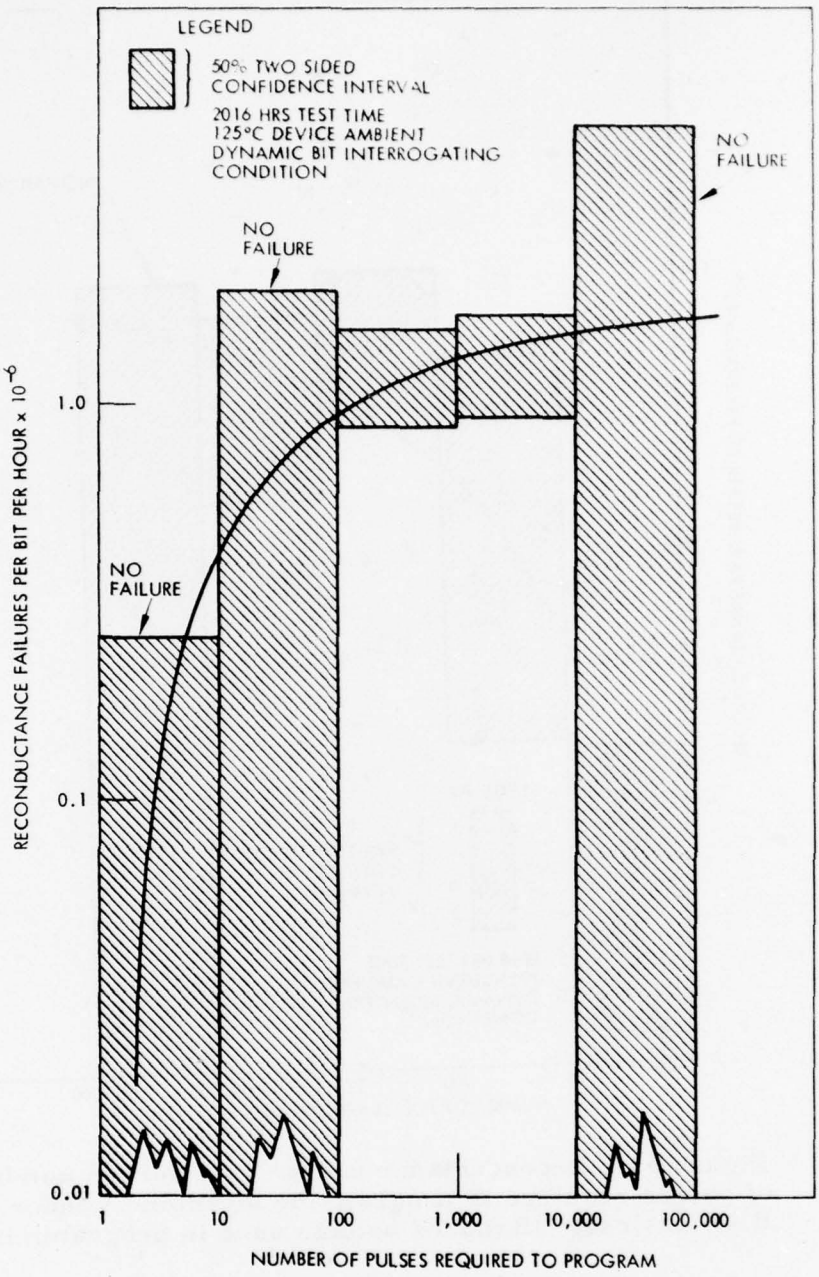

Figure 40. Reconductance failure rate versus number of pulses required to program for nichrome vendor A 1K devices. (Reduced voltage used in programming.)

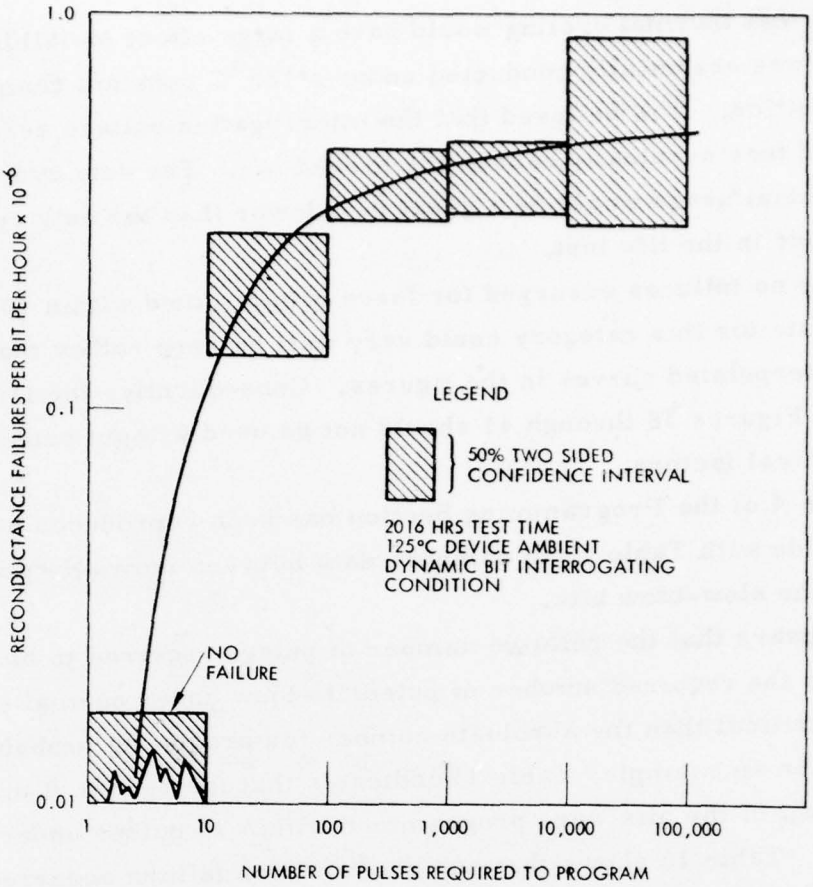

Figure 41. Composite reconductance failure rate versus number of pulses required to program for all nichrome devices. (Vendors A and B, and 1K, 2K and 4K devices; reduced voltage used in programming.)

widths, voltages and shapes are different for these two vendors. Merging the data according to the number of pulses required to program would have a smoothing effect on the curves. For example, if the knees of the individual curves were different, the merged curve then would have a softer knee.

The life test was conducted at 125°C. The failure rates at lower temperatures such as a 25° to 50°C could be several order of magnitude lower than the 125°C figure. Although a fuse is like a resistor, the failed portion of a programmed fuse is an insulator. This insulator would be akin to the insulation in some types of capacitors such as electrolytic, glass or ceramic. Temperature greatly affects the failure rates of these capacitors. It is also

believed that thermal cycling would have a large effect on failure rate. The life test was essentially conducted under a 125°C constant chamber temperature condition. It is believed that the interrogation voltage across the programmed fuse eventually causes the breakdown. The duty cycle of interrogation in actual usage would be a great deal lower than the duty cycle of interrogation done in the life test.

Since no failures occurred for fuses programmed within 10 pulses, the failure rate for this category could very well be zero rather than indicated by the interpolated curves in the figures. Consequently, the failure rate shown in Figures 38 through 41 should not be used without consideration for other critical factors.

Table 4 of the Programming Section has been reproduced here as Table 17 side by side with Table 16 to compare data between normally programmed bits and the slow-blow bits.

It appears that the relative number of pulses required to blow with respect to the required number of pulses to blow under normal conditions is more critical than the absoluate number for predicting probability of failure. As an example, Table 17 indicates that for vendor B nichrome 1K devices, all of the bits were programmed within 10 pulses under the normal condition. Table 16 shows that one reconduction failure occurred for the group programmed between 10 and 100 pulses and more failures occurred for the higher pulse count categories. On the other hand, the 2K devices of vendor B had bits that required a large number of pulses (some over 10,000 pulses) to program for the normal condition (Table 17) and only one failure occurred in the over 10,000 pulses category (Table 16.) The polysilicon PROMs exhibited similar behavior. The 1K and 4K devices of vendor X required a larger number of normal pulses to program. No reconductions were experienced on these parts. However, the 2K devices of vendor X showed requirements of fewer numbers of normal pulses to program (Table 17) and failures began to occur for bits purposely programmed with greater than 1000 pulses (Table 16). One explanation might be that the manufactured fuse properties (sheet resistances, cross-section, etc.) determine their basic programming characteristics, i.e., number of pulses to blow under normal condition. The relative figure for number of pulses with respect to the

TABLE 16. COUNTS OF NUMBER OF BIT REVERSALS AFTER 2016 HOURS, 125°C LIFE TEST AND COUNTS OF NUMBER OF BITS PROGRAMMED WITH REDUCED PULSE VOLTAGES AS WELL AS NORMAL PULSE VOLTAGE

Technology	Manufacturer	Device Capacity (Bits)		Categories according to number of pulses required to program				
				1 to 9	10 to 99	100 to 999	1000 to 9999	Over 10,000
Nichrome	B	1K	No. of Bit Reversals	0	1	1	4	2
			No. of Bits Programmed	6245	871	1214	1275	687
		2K	No. of Bit Reversals	0	0	0	0	1
			No. of Bits Programmed	4822	5695	4140	2838	937
		4K	No. of Bit Reversals	0	1	5	3	0
			No. of Bits Programmed	10862	2178	3592	3149	699
	A	1K	No. of Bit Reversals	0	0	9	8	0
			No. of Bits Programmed	2669	364	3863	3206	138
		2K	No. of Bit Reversals	0	4	0	0	0
			No. of Bits Programmed	5318	5378	4114	3371	251
		4K	No. of Bit Reversals	0	0	0	0	0
			No. of Bits Programmed	10583	818	3444	5424	211
Polysilicon	X	1K	No. of Bit Reversals	0	0	0	0	0
			No. of Bits Programmed	0	0	7773	276	660
		2K	No. of Bit Reversals	0	0	0	2	1
			No. of Bits Programmed	650	4079	4183	10398	1170
		4K	No. of Bit Reversals	0	0	0	0	0
			No. of Bits Programmed	0	10	16479	2579	1412

(Table 16, concluded)

Technology	Manufacturer	Device Capacity (Bits)		Categories according to number of pulses required to program: 1 to 9	10 to 99	100 to 999	1000 to 9999	Over 10,000
AIM	Y	1K	No. of Bit Reversals	0	0	0	0	0
			No. of Bits Programmed	2580	2192	1316	3228	924
		2K	No. of Bit Reversals	0	0	0	0	0
			No. of Bits Programmed	3715	1780	4558	9272	1155
		4K	No. of Bit Reversals	0	0	0	0	0
			No. of Bits Programmed	6867	1754	6409	840	513

TABLE 17. DISTRIBUTION OF NUMBER OF BITS PROGRAMMED *WITH VENDOR RECOMMENDED METHODS* AS A FUNCTION OF PULSES TO PROGRAM

Technology	Manufacturer	Device Capacity (Bits)	Number of Bits: Categories according to number of pulses required to program: 1 to 9	10 to 99	100 to 999	1000 to 9999	Over 10,000
Nichrome	B	1K	6044	0	0	0	0
		2K	4631	3474	1785	337	13
		4K	10024	207	9	0	0
	A	1K	2560	0	0	0	0
		2K	5120	0	0	0	0
		4K	10240	0	0	0	0
Polysilicon	X	1K	0	0	6076	66	6
		2K	354	3717	1049	0	0
		4K	0	10	10225	5	0
AIM	Y	1K	2048	1002	22	0	0
		2K	3715	1405	0	0	0
		4K	6796	1395	0	0	0

normally required number of pulses is a measure of how much current reached the fuse. In other words, the current starved condition of a fuse blown with 1000 pulses is a group that normally blows for 100 pulses is the same as one blown with 100 pulses in a group that normally blows for 10 pulses. If this explanation is correct then manufacturing variations could greatly modify the failure rate curves with respect to the absolute values of number of pulses to program. The shape of the curves however, should remain the same. It is important to note that the key factor for blowing a fuse is energy which can be applied by means of multiple short pulses or a single long pulse.

Based on these results, it appears to be important to place a limitation on the allowed number of pulses used to program a fusible link, keeping in mind that the limits could change when the chip design changes. A decision on the exact number of pulses permitted would be the result of a trade-off between cost and reliability, since decreasing the number of pulses will adversely affect the programming yield while increasing it will result in a higher operational failure rate. Extensive programming yield and field failure data would be required to exactly quantify this trade-off. The data shown in curves such as that of Figure 41 reflect the worst - worst case conditions of continuous high temperature operation and maximum interrogation voltage application and as such the absolute failure rates displayed are extremely pessimistic and cannot be used directly to quantify the trade-off. However some conclusions as to relative failure rates can be drawn. Since the completion of the first HAC PROM evaluation[2] extensive progress has been made in the area of Nichrome PROM technology. Most of the fuses of the newly designed parts from Harris and MMI can be blown with a single 100 μs pulse. This is quite contrary to the earlier parts which required millisecond pulses to program. Furthermore, the circuit breakdown problem due to fast risetime of the programming pulse also does not exist in the new parts. Therefore the old recommendation of using millisecond pulses with no longer than 100 μs risetimes is no longer applicable. Referring to the curve in Figure 41, it appears that for NiCr PROMs the 10 pulse level may be taken as a break point. A limitation of ten pulses would produce a failure rate reduction of five to one over unrestricted programming. This represents a level not to be exceeded and should only be used in

non-critical applications. It is to be noted that this selection of a maximum of 10 pulses is not a black and white decision. For example if 20 pulses were used only a few percent more failures would occur. Reducing the allowed number even further will rapidly decrease the relative failure rate with a 50 to 1 reduction predicted for a very few pulses. The best approach would seem to be to reduce the pulse limit to as low a level as reasonable programming yield considerations will permit. At the present time perhaps a fair judgment would be to allow 10 pulses in non-critical applications and to reduce the limit to one or two pulses for high reliability applications. The method of two pulses would be to hit each fuse with one pulse and then those that did not program the first time with a second pulse. Each vendor has its own unique PROM design. The way programming current is directed to the fuse and the required fusing energy differ between vendors. It is important that the vendor recommended pulse shapes be used for programming.

While the above paragraph discussed the case for NiCr PROMs, the same reasoning applies for polysilicon PROMs except that as many as 1000 pulses should be permitted as evidenced by the number of pulses normally required to program (Table 17) and the failures which occurred for only bits programmed with higher than 1000 pulses (Table 16).

Since no failures were experienced for AIM PROMs programmed with large number of pulses, no maximum number of programming pulses need be set for AIM PROMs.

8. SCREENING TESTS

Programmable read-only memories are one type of microelectronic device. As such, they are subject to the screening for all microelectronics specified in MIL-STD-883, Method 5004. Additional screening tests are sometimes specified in the MIL-M-38510 detail specifications (slash sheets). The details of various tests and analyses pertinent to screening are contained in the sections on Programming, Memory Element Failure Mechanism, and Burn-In and Life Tests. The use of such additional tests is scussed below for each of the PROM technologies.

CORROSION RESISTANCE SCREENING (CRS) TESTS

CRS Tests for Polysilicon Fuse PROMs

For NiCr fuse link PROMs, an additional screening test, the freeze-out test, a Group B inspection test, and the water drop test are specified to test the adequacy of the passivation overglass. These tests should not be necessary for polysilicon fuse link PROMs because polysilicon is resistant to corrosion, due to its self-passivating oxide, and because the amount of material in the fuse link is much larger than in the case of NiCr fuses. However, the overglass passivation is removed from every polysilicon fuse link during manufacturing in order to facilitate programming. Therefore the freeze-out and water drop tests were performed on some polysilicon fuse devices to verify that corrosion is not a threat to these devices, as described in the section on failure mechanisms. No corrosion of polysilicon was detected in those tests, so there is no apparent reason for special screening tests of the corrosion resistance of these devices.

No other special screening tests were investigated for polysilicon fuse PROMs and none is recommended.

CRS Tests for AIM PROMs

No additional screening tests have been specified in MIL-M-38510/202, the detail specification for 1024-bit AIM devices. None were found to

warrant investigation during this study and no test in addition to Method 5004 is recommended as a result of this study.

CRS Test for NiCr Fuse PROMs

The current detail specification for 512-bit NiCr PROMs, MIL-M-38510/201, specifies a screening test, the freeze-out test (paragraph 4.3e), in addition to Method 5004. This test is intended to evaluate the moisture content inside the device package and the adequacy of the passivation glass which is supposed to protect the NiCr fuse links against corrosion, as well as provide mechanical protection to the circuit. Corrosion of an unprogrammed fuse link would result in its conversion to an apparently programmed link and thus failure of the device. Since there have been failures of this type reported[2] and there were similar problems with NiCr resistors in other applications, the addition of the freeze-out test was a reasonable precaution. However, it does require time and expense to perform, so its use merits reevaluation.

All of the nine NiCr PROMs put through the freeze-out test during this study (see the section on failure mechanisms of this report) passed that test. Furthermore none had any NiCr failures during the more severe water drop test. Inspection of these devices did not reveal any cracks in the passivation glass edges of the Al metallization lines where they contact the NiCr. Thus the passivation glass appears to be effective in the devices examined. However, the small number of devices included here does not allow any valid determination of the overall need for the freeze-out test.

The water drop test of the Group B inspection (paragraph 4.4.2(c) of MIL-M-38510/201) is also intended to evaluate the passivation integrity of each lot of Class A devices. If no failures of the freeze-out test have occurred for recent lots which passed the water drop test, then the possibility of dropping the freeze-out test for Class A devices should be considered. On the other hand, it would not be appropriate to delete the water drop test and retain only the freeze-out test for Class A devices, as is done for Class B and Class C devices (paragraph 4.4.3f). This is because the freeze-out test requires two factors for failure: a dew point inside the

package of -10°C or above and a defect in the passivation glass over a NiCr fuse link. If a device passes this test only because of a low dew point, moisture may subsequently leak into the package and cause a failure by corrosion through passivation defects. If the lot from which that device was drawn had been subjected to the water drop test the defective glass passivation that permitted the subsequent failure could have been detected and the lot rejected initially.

No other screening tests in addition to those in Method 5004 were investigated during this study and none in addition to the freeze-out and water drop tests is recommended for the NiCr fuse technology.

BURN-IN SCREENING TESTS

A question frequently arises as to whether burn-in should be performed before or after programming of fusible link PROMs. In situations where the user stockpiles parts which he would later program according to need, logistics are simplified by a pre-programming burn-in, perhaps performed by the vendor. However, in view of the results of this study, as reported in the Burn-In and Life Test Section, this increases the probability that an improperly programmed fuse might go undetected and be sent into the field. It is therefore recommended that burn-in be performed after programming, at least until experience clearly establishes that control of programming parameters and limitation of the allowed number of programming pulses will eliminate the possibility of an improperly programmed fuse.

Based on analyses reported in the section on Burn-In and Life Tests, a 168 hr., 125°C burn-in could weed out 60 to 70 percent of the parts that might fail because of insufficient current reaching the fuses during programming. Note that the insufficient current conditions were purposely imposed in this study to induce failures. For the AIM devices, no failures were experienced during the life test. There is no data on the AIM devices to substantiate pro or con with respect to the standard burn-in time. It is recommended that the standard MIL-STD-883 burn-in times remain unchanged. The burn-in should be done after programming for fuse link type PROMs. For AIM type PROMs it may be done either before or after programming.

TEMPERATURE SCREENING TESTS

In specifying the functional testing to be performed, consideration should be made of the temperature dependent behavior of marginally programmed fuses (see section on Burn-In and Life Tests). It is frequently observed during this study that devices programmed and tested at room temperature do not necessarily operate properly over the full military temperature range.

This is true of devices utilizing AIM technology as well as fusible link devices. In the case of the AIM devices, this may be due to the fact that these devices, which are programmed in an incremental fashion, depend on correlation of the special verification procedure used during programming to assure proper functional performance over the full temperature range. The verification reference point might not provide sufficient margin to assure full temperature range operation.

While it may be possible to devise more stringent room temperature tests which assure full temperature range operation, at present functional testing at the temperature extremes is an important safeguard against the deployment of improperly programmed devices. 100 percent full temperature tests are recommended for all of the device types covered in this study if no temperature screening will be done at the assembly level.

9. SUMMARY, CONCLUSIONS AND RECOMMENDATIONS

The pertinent findings, conclusions and recommendations for the three PROM technologies studied are summarized in Tables 18 - 20.

TABLE 18. POLYSILICON FU

Memory Element	This technology uses as memory elements fuse links of polycrystalline silicon material. The fuses are approximately 0.35 μm thick and 2.2 μm wide at the neck. To facilitate programming, the passivation glass is removed at the fuse locations. Thus the fuses are exposed to the atmosphere of the device cavity. The unprogrammed fuse link resistance is approximately 100 ohms. When programmed the fuses are blown via electric current to an open condition of greater than one meg-ohm. The minimum resistance for a fuse to appear programmed is in the 1000 ohm region.
Programming	Programming pulse widths beginning with 1 μs and then increasing linearly to 8 μs maximum in 100 ms are used in standard programming. 99.64 percent of the fuses were programmed within 1000 pulses. Programming yields of 97 percent and 90 percent were reported by users for the 1K and 2K devices respectively using multiple pulses. It is recommended that a maximum of 1000 pulses be allowed for programming devices from this technology. Vendor recommended pulse shapes should be used.
Programming Mechanism	After the programming current melts the polysilicon fuse, its surface tension pulls it into a few rounded lumps at the center of the fuse. Subsequently, the thinned region between the central lumps and the emitter end of the fuse opens. This results from the migration of silicon away from that region under the influences of the electric field and the thermal gradient in that region. Oxidation of the hot silicon may also contribute to interrupting the electrical conductivity of the fuse. The apparent gaps in the programmed fuses are very narrow.
Memory Element Failure Mechanisms	The polysilicon fuse is self-passivating and is not as liable to corrode as some other fuse links. Its thickness also helps to resist any corrosion damage. Freeze-out and water drop tests did not cause failures even though the fuses were not protected by any passivation layer. However, the exposed fuses are subject to the hazard of loose particles inside the package, shorting adjacent

LE 18. POLYSILICON FUSE TECHNOLOGY

		elements. Reconduction of programmed fuses has been reported in the industry. By limiting current, a marginal fuse can be created that would reconduct after operation for some time. Such marginal fuses showed very narrow gaps. Reconduction may result from conductance through the thin dielectric in the narrow gap at high temperatures and finally electrical breakdown. Melting is possibly involved at the end to form a permanent reconduction.
	Burn-In and Life Tests	A 2016 hour, 125°C life test was conducted on ten 1K, ten 2K and five 4K devices. The bits in these devices were programmed in two groups. Group I was programmed with vendor recommended method and Group II was programmed with reduced pulse voltage to induce marginal fuses. No failures were experienced in the Group I fuses. The Group II fuses showed failures in two devices with a total of three fuse failures. All of the failures occurred prior to 168 hours of test. Some reconducting fuses would occasionally open again, indicating that these fuses were probably in a marginal condition. None of the bits programmed under 1000 pulses failed.
	Screening Tests	The special freeze-out test and water drop test are not applicable to this technology and should not be used. The standard MIL-STD-883, Method 5004 tests should be conducted. Burn-in time of 168 hours at 125°C with dynamic addressing should suffice. The burn-in should be done after programming. Full military temperature range testing after programming should be done until sufficient information exists to prove otherwise.

TABLE 19. AVALANCHE-INDUCED

Memory Element	This technology uses floating base *n-p-n* transistors as memory elements. The base thickness is approximately 0.3 μm. The military AIM devices are passivated with a 1 μm thick CVD overglass of a sandwich structure of SiO_2, P-SiO_2 and SiO_2. The resistance of the unprogrammed element is approximately 10^9 ohms. When programmed the emitter-base junction is blown via electric current to a short condition of less than 10 ohms.
Programming	Programming current pulse width of 7.5 μs is used in standard programming. 99.87 percent of the memory elements were programmed within 100 pulses. Programming yield of 96 percent was reported by a large quantity user for 1K devices using standard multipulse programming. It is recommended that no limitation be placed on the total number of pulses used for programming.
Programming Mechanism	The programming mechanism involves rapid migration of Al from the emitter contact through the emitter-base junction. This migration occurs at a hot spot where most of the electric current passes through the reverse biased emitter-base junction simultaneously. Si diffuses out of the emitter region into the Al emitter contact because of the concentration gradient. After the junction is shorted by the Al "finger," the region cools rapidly, preserving the inhomogeneous structures observed as white lumps on emitter contacts and Al "fingers" in sectioned devices.
Memory Element Failure Mechanisms	Possible failure mechanisms are growth of alloying pits to short the emitter-base junction of an unprogrammed element or the further diffusion of the aluminum spike through the collector-base junction of a programmed element. However, no failures related to the first failure mechanism have been reported. The second failure mechanism may not be a problem because the aluminum spike diffusion may only increase the local carrier concentration of the p-type base region and push the base-collector junction further into the collector without causing a short. There have been no definitive memory element failures reported in the industry.

p-n e base thick- nilitary AIM ick CVD SiO_2, P-SiO_2 ogrammed When pro- blown via of less than	Burn-In and Life Tests	A 2016 hour, 125°C life test was conducted on ten 1K, ten 2K and four 4K devices. The bits in these devices were programmed in two groups. Group I was programmed with the vendor recommended method and Group II was programmed with reduced current pulse amplitude to attempt to induce marginally programmed memory elements. No failures were experienced for elements programmed in either group. Another special life test of 1147 hours at 125°C was performed on one device with 11 elements programmed to verification voltages of 5.1 to 8.0 volts to study the stability of the resistance of the programmed elements. The verification voltage is a measure of the element resistance. The variations on the verification voltages during this life test ranged from 1.2 to 21 percent, which is not high enough for concern.
7.5 μs is 17 percent of ned within 5 percent for 1K ogramming. be placed on rogramming.		
es rapid ntact through ration occurs ric current nitter-base out of the ontact because the junction gion cools us structures contacts and	Screening Test	No tests other than the standard MIL-STD-883, Method 5004 tests are recommended. Burn-in times should follow standard practice for semiconductors. Burn-in may be done either before or after programming. Full military temperature range testing after programming should be done until sufficient information proves otherwise.
owth of alloy- nction of an r diffusion llector-base However, no nechanism lure mechan- he aluminum e local carrier ion and push nto the collec- have been no reported in		

TABLE 20. NICHROME FUSE

Memory Element	This technology uses fuse links of nichrome material as memory elements. The fuses are typically about 200 nm thick and 4 μm wide at the neck. Ni:Cr ratio and dimensions vary among manufacturers. The fuses and the overall chip surface are typically protected by a layer of phosphosilicate glass 1 μm thick. The typical unprogrammed fuse link resistance is 400 ohms. When programmed, the fuses are blown to an open condition of greater than one meg-ohm. The minimum resistance for a fuse to appear programmed is in the 4000 ohm region.	Burn Test
Programming	Programming pulse widths of 67 μs and 100 μs were used. A sawtooth waveform was used with the 67 μs pulse. All of the fuses programmed within 10 pulses for one vendor. For the other vendor 78 percent of the fuses programmed within 10 pulses. Programming yields of 85 to 95 percent were reported by large quantity users for 1K and 2K devices using multiple pulses. Small quantity experiment by a user experienced 50 to 80 percent yield on 2K devices using single pulse programming For non-critical usage a maximum of 10 pulses may be used. Vendor recommended pulse shapes should be used.	
Programming Mechanism	Investigation by Kenney, Jones and Ogilvie has resulted in a detailed description of the programming mechanism. This involves melting of the NiCr film by Joule heating, expansion of holes in the liquid film due to its surface tension, and breakup of the perameters of the holes by perturbations, resulting in symmetrical filaments of NiCr in the fuse gap. The filaments may in turn break into droplets. The spinel (oxide) film left in the gap may also melt and break up in a similar fashion.	Scre
Memory Element Failure Mechanisms	Two failure mechanisms were identified in the earlier study, namely corrosion of the fuses caused by water penetrating through the passivation layer and reconduction of programmed fuses. There have been no failures due to corrosion reported by the industry in the last two years. However, there were reconduction failures reported. By limiting current to a fuse a marginal fuse can be created that would reconduct after operation for some time.	

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material lly about :Cr ratio The ally pro- µm thick. nce is re blown to ohm. The rogrammed	Burn-In and Life Tests	A 2016 hour, 125°C life test was conducted on 21 1K, 19 2K and 10 4K devices, with the devices roughly divided equally between the two vendors utilized. The bits in these devices were programmed in two groups. Group I was programmed with vendor recommended methods and Group II was programmed with reduced pulse voltage to induce marginal fuses. No failures were experienced in the Group I fuses. The Group II devices showed 35 fuse failures in 17 devices. 65 percent of the device failures occurred prior to 168 hours of test and 94 percent prior to 336 hours. Some reconducting fuses would occasionally become open again, which indicates that these fuses were probably in a marginal condition. None of the fuses programmed within 10 pulses failed. Cumulative fuse failure curves were analyzed. The curve for 1K devices showed a knee around 250 hours of test and the curves for 2K and 4K devices showed knees around 500 hours. This phenomenon agrees with the reconduction theory of dielectric breakdown developed in the earlier study. In this theory the time to failure varies inversely as the applied voltage and the length of time the voltage is applied. The voltage stress in this case is the interrogation voltage. Due to the word organization, the duty cycle of the interrogation voltage on the bits of the 2K and 4K devices is one half of that of the 1K device.
µs were the 67 µs 10 pulses ercent of rogram- ed by large multiple er experi- using single		
of 10 pulses shapes		
has ogramming NiCr film liquid film the peram- ing in gap. The The spinel nd break up	Screening Tests	The MIL-STD-883, Method 5004 tests, the freeze-out test and the water drop test should be continued for this technology. Burn-in time of 168 hours at 125°C with dynamic addressing could weed out 65 percent of the marginal fuses. Extending the burn-in times to 240 hours for Class B devices might be desirable. However, from a practical and standardization view point it is recommended that the Method 5004 standard be maintained. The burn-in should be done after programming. Full military temperature range testing after programming should be done until sufficient information proves otherwise.
the earlier ed by water nd recon- been no ndustry in reconduction a fuse a conduct		

10. RECOMMENDATIONS FOR FUTURE STUDY

Pertinent information has been derived from this study to qualitatively indicate that the specific parts utilized from the three technologies (polysilicon fuse, nichrome fuse and AIM) have reasonable programming yield and reliability characteristics; and fuse reconduction failures can be aggravated by limiting programming currents to the fuses and high temperature operation of devices. To project this information for use with PROMs programmed and operated under standard conditions, further study on a large sample basis will be required. There are many more types of PROMs now available in the market. Similar evaluations should be done on these new types to assess their reliability before actual usage in production systems. The following are recommendations on future studies.

1. Large Sample Correlation Study

   During the present study, fuse type PROMs with long blow times, which were blown with low programming currents, were found to be associated with higher reconduction failure rates. In order to verify this with normal programming methods, a study may be conducted with a large number of PROMs programmed with standard methods. In this study the number of pulses required to program each fuse should be recorded. The PROMs are then operated under normal conditions. The recorded failures are then correlated back to the number of pulses to program data. The output of this study will give both programming yield data and failure rate data as functions of number of pulses to program. This study can best be done by firms that are already using large quantities of PROMs and are logging the operating time and failures.

2. Burn-In Study

   For fuses blown with reduced currents, the 125°C burn-in time appeared to be optimal around 250 to 500 hours. In order to verify this optimum time for fuses blown with standard methods a large amount of test information needs to be collected. Such information is available in the Group B Life Test data from the manufacturers. The Life Test data should be collected and analyzed for both optimum burn-in time determination and failure rate determination.

3. Accelerated Tests on AIM PROMs

   The present study indicates that the memory elements of AIM PROMs have relatively few failure mechanisms, and that these mechanisms are insensitive to programming variations. Thus it

has the potential of being a PROM that can be programmed with sloppy setup and still achieve high reliability. The two possible failure mechanisms, alloying pit growth and aluminum spike diffusion, may in truth not be potential problems at all. By means of accelerated tests such as high temperature test coupled with various programming procedures, the seriousness of these possible failure mechanisms can be determined.

4. Evaluation of Other Types of PROMs

So far only PROMs that are irreversibly programmed have been evaluated. There is a whole family of PROMs that are erasable and reprogrammable for large numbers of times. These PROMs (FAMOS, MNOS, etc.) can be erased electrically, or by ultraviolet light. Usually these PROMs depend on a stored charge to hold a programmed bit. If the charge should leak, the bit would eventually change. Therefore the failure mechanisms for these PROMs are quite different from those studied. More and more of these PROMs are coming into use. It is important that their reliability be evaluated before actual usage in production systems.

APPENDIX I

USER INFORMATION SURVEY FORM

PROM Reliability Information Collection Form

(Please use one form for each part type)

1.1 Generic PROM family: ☐ NiCr Fuse; ☐ Si Fuse; ☐ TiW Fuse; ☐ AIM

1.2 No. of bits: ☐ 256: ☐ 512; ☐ 1K; ☐ 2K; ☐ 4K; ☐ 8K.

1.3 Manufacturer: _____ Part No.: _____

1.4 Quality level of parts: ☐ Commercial; 38510 or equivalent ☐ A; ☐ B; ☐ C.

2.1 No. of parts programmed: _____ When: _____

2.2 Programmed by: ☐ Manufacturer; ☐ Distributor; ☐ User

2.3 Programming method: ☐ Mfg.'s Standard; ☐ Other (Please describe below).

2.4 Do you limit programming to: ☐ One pulse; ☐ Others___; ☐ No limit.

2.5 Programming equipment used: _____

2.6 Chip usage - rough percentage of bits per part required to be programmed _____ %.

2.7 Programming Yield: _____ % (Part basis)

3.1 Tests Conducted: (Please describe screening, life or other test conditions, test times, number of parts tested, when tests were conducted, etc.)

3.2 Failures experienced from tests: (Please describe symptoms, when failures occurred, functional test condition, etc.)

3.3 Failure analysis results: (Please describe failure analyses, measurements, etc.; attach photo if available.)

4.0 Field or usage experience: (Operating conditions, operating time, failures, failure analyses, quantity of parts used, etc.)

5.1 Your name:_____ Title:_____

Company:_____

Address:_____

_____ Zip Code

Telephone: ( )_____

6.0 Normally we do not publish data sources in the report unless permission is obtained from the contributors.

6.1 Would you want your name mentioned as contributor: ☐ yes; ☐ no

6.2 Would you want your name associated with this data: ☐ yes; ☐ no

6.3 Would your company want to have its name associated with this data: ☐ yes; ☐ no

7.0 Other information you wish to supply:

APPENDIX II

CONTRIBUTORS OF PROM USER INFORMATION

Acknowledgement is given to the following individuals who have contributed valuable information utilized in this study.

Jack Craig, Lockheed Missile and Space Company, Sunnyvale, California

Howard Gerwin, Sandia Laboratories, Albuquerque, New Mexico

H. Y. Ho. Xerox Corp., El Segundo, California

Roger S. Mo, Xerox Corp. El Segundo, California

Roger Mobley, Collins Radio, Cedar Rapids, Iowa

Dave O'Connor, General Electric, Pittsfield, Mass.

Dale Platteter, Naval Weapons Support Center, Crane, Indiana.

Robert Raichlin, Hughes Aircraft Company, Culver City, California

APPENDIX III

VENDOR RECOMMENDED PROGRAMMING METHODS

ROM AND PROM PROGRAMMING INSTRUCTIONS

11. Manually Programming the 3601 (or 3601-1)

The 3601 may be programmed using the basic circuit of Figure 1. Address inputs are at standard TTL levels. Only one output may be programmed at a time. The output to be programmed must be connected to V_{CC} through a 300Ω resistor. This will force the proper programming current (3-6mA) into the output when the V_{CC} supply is later raised to 10V. All other outputs must be held at a TTL low level (0.4V).

The programming pulse generator produces a series of pulses to the 3601 V_{CC} and $\overline{CS}_2$ leads. V_{CC} is pulsed from a low of 4.5 ± .25V to a high of 10 ± .25V, while $\overline{CS}_2$ is pulsed from a low of ground (TTL logic 0) to a high of 15 ± 0.5V. It is important to accurately maintain these voltage levels, otherwise, improper programming may result. The pulses applied must maintain a duty cycle of 50 ± 10% and start with an initial width of 1 (± 10%)μs, and increase linearly over a period of approximately 100ms to a maximum width of 8 (± 10%)μs. Typical devices have their fuse blown within 1ms, but occasionally a fuse may take up to 400ms. During the application of the program pulse, current to $\overline{CS}_2$ must be limited to 100mA. The output of the 3601 is sensed when $\overline{CS}_2$ is at a TTL low level output. A programmed bit will have a TTL high output. After a fuse is blown, the V_{CC} and $\overline{CS}_2$ pulse trains must be applied for another 100μs. One circuit which can be used to generate this pulse train is shown in Figure 2, while the characteristics of the pulse train are shown in Figure 3.

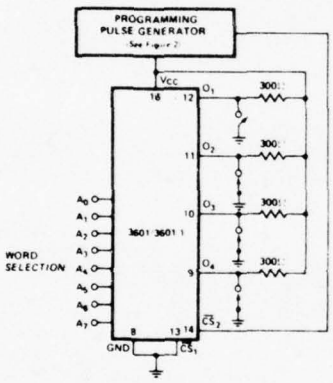


Figure 1. 3601 Programming

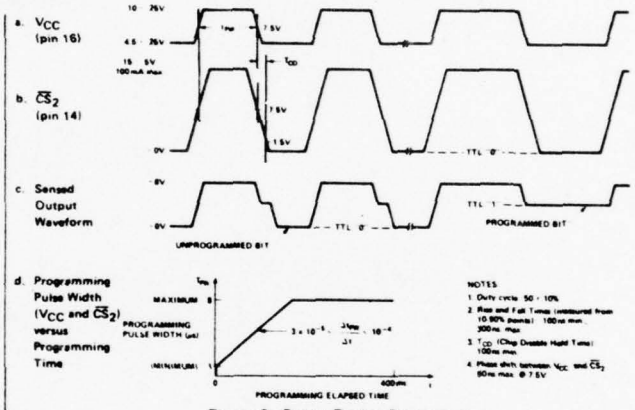


Figure 3. Pulses During Programming

ROM AND PROM PROGRAMMING INSTRUCTIONS

III. Manually Programming the 2K and 4K Bipolar PROMs

The Intel 2K and 4K bipolar PROMs may be programmed using the basic circuit of Figure 1. Initially all bits (either 2048 or 4096) are in a logic 1 (high) state. Only one output may be programmed at a time. The programming current (5mA ±10%) is forced into the output to be programmed by a current source. The current should be clamped to V_{CC} by a silicon diode. All other outputs must be allowed to float such that the outputs are allowed to rise one diode above V_{CC} (12.5V).

For simplicity of the programming description, reference will be made only to V_{CC}, however, this term includes both the V_{CC1} and V_{CC2} of the 4K PROM. There is only one V_{CC} for the 2K PROM. Programming pulses must be applied to both V_{CC} and $\overline{CS}$. A series of pulses is applied to the V_{CC} and $\overline{CS}_1$ leads as shown in Figure 3a and 3b respectively. The pulse applied must maintain a duty cycle of 50 ±10% and start with an initial width of 1 (±10%) μs, and increase linearly over a period of approximately 100ms to a maximum of 8 (±10%) μs. Typical devices have their fuse blown within 1ms, but occasionally a fuse may take up to 400ms. During the application of the program pulse, the V_{CC} current must be limited to 600mA and the $\overline{CS}_1$ current to 150mA. A programmed bit will have a TTL low level. After a fuse is blown, the V_{CC} and $\overline{CS}_1$ pulse trains must be applied (the pulse width still linearly increasing to a maximum of 8μs) for another 100μs.

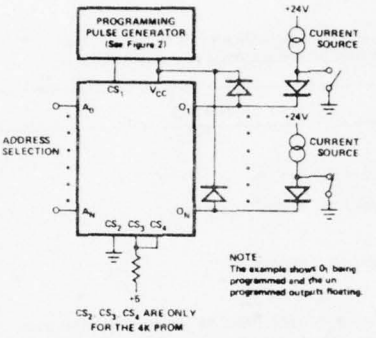


Figure 1. 2K and 4K Bipolar PROM Programmer

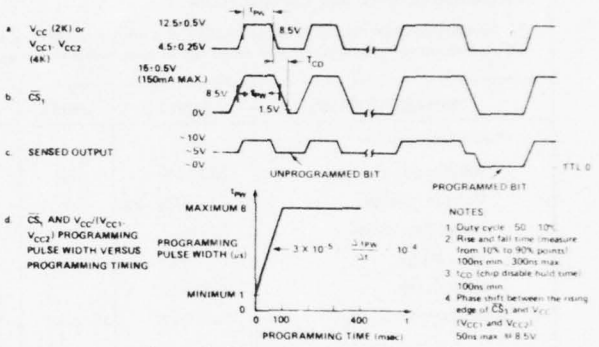


Figure 3. Pulses During Programming

For 1K and 2K devices

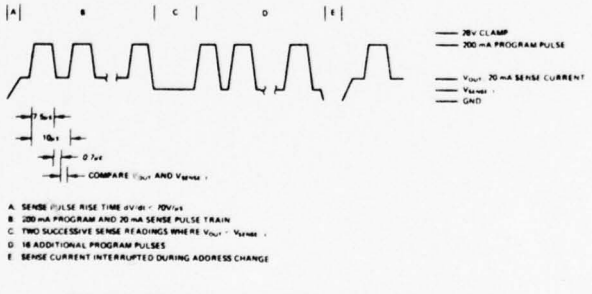
PROGRAMMING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V)

SYMBOL	CHARACTERISTICS	TYP	UNITS	CONDITIONS
t_{PR}	Time to Electrically Alter a Bit at Logic "0" to Logic "1"	200	μs	Using INTERSIL, INC. Programming Equipment

PROGRAMMING SPECIFICATION

To correctly program the IM5603A or IM5623, it is imperative that this specification be rigorously adhered to. Intersil, Inc., will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

CHARACTERISTICS	LIMIT	UNITS	NOTES
Programming Pulse:			
Amplitude	200 ±5%	mA	Constant Current
Voltage (clamp)	28.0 +0% -2%	V	Voltage limit of current source.
Ramp Rate dv/dt	70 max.	V/μs	
Pulse Width	7.5 ±5%	μs	15V points, 150Ω load
Duty Cycle	70% min.		
Sense Current	20.0 ±0.5	mA	The sense current must be interrupted after each address change for 10μs min. The sense current ramp rate dv/dt must be <70V/μs, and clamped to 28.0V +0% -2%.
Programming V_{CC}	5.0 +5% -0%	V	
Maximum Sensed Voltage for a programmed "1"	7.0 ±0.1	V	A bit is programmed when two successive sense readings 10μs apart with no intervening programming pulse, pass the limit. When this condition has been met, 16 additional program pulses are applied and the pulse train is then terminated.
Delay from trailing edge of program pulse before sensing output voltage.	0.7 min	μs	



TYPICAL VOLTAGE WAVEFORM DURING PROGRAMMING

NOTE: For information on programming a number of IM5603A or IM5623 units mounted on a board, contact Intersil.

For 4K devices

IM5605A, IM5625 PROGRAMMING CHARACTERISTICS

PRELIMINARY PROGRAMMING SPECIFICATION

CHARACTERISTIC	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNITS	CONDITIONS
Programming Current Pulses	190	200	210	mA	Constant current to be supplied over a 10V to 28V range. Set nom. value with 100Ω, 6W load @ +20V.
Voltage Clamp (for constant current source)	27.5	28	28.5	V	Constant voltage clamp is adjusted when sinking constant current of 200 ma nom. value (external load disconnected)
Rise rate dv/dt (program current source)	50	60	70	V/μs	Voltage rise rate is measured by switching from 20 to 200 ma into a 200Ω, 6w, resistor with the maximum voltage clamped at 28V
Pulse width	7.0	7.5	8.0	μs	Measured at 10V points when switching between 20 and 200 ma into a 100Ω, 6w load resistor
Sense Width	2.0	2.5	3.0	μs	Measured at 10V points when switching between 20 and 200 ma into a 100Ω, 6w load resistor. Measure from trailing edge to leading edge on the program pulse (Refer to timing diagram)
Sense Voltage (Analog Comparator Reference Voltage)	6.9	7.0	7.1	V	An element is considered programmed when the voltage sensed at the bit output pin with 20 ma forced is less than the analog comparator reference voltage
Sense Current (Amplitude)	19.5	20.0	20.5	ma	Constant current source amplitude is adjusted for a nominal value of 20 ma into a 12V, 400mw, zener diode. (Refer to timing diagram for 20 ma control)
Ramp Rate dv/dt (sense current source)	50	60	70	V/μs	Voltage rise rate measured by switching from 0 to 20 ma into a 1.5K, 1w resistor with the max. voltage clamped at 26 volts
Delay from trailing edge of programming pulse before sensing	9	10	11	μs	Measured from the 10V level of the voltage pulse when switching from 200 to 20 ma into a 100Ω, 6w load resistor.
Programming V_{CC}	4.9	5.0	5.5	V	V_{CC} to the part under programming. Limit current to 200 ma
Programming Time Allocation/Bit		10		ms	Maximum time allowed to program a bit
Extra Programming Pulses		4		pulses	Absolute number of programming pulses to be issued after the bit output is first sensed as a programmed "1". This occurs when the sensed voltage is less than the comparator reference voltage.

PIN CONDITIONING

Chip enable (pin 20 & 21) High (de selected) during programming, ground for logical verify.
Chip enable (pin 19 & 18) High (selected) during programming and logical verify.
P_{VCC} (pin 22) to V_{CC} during programming and ground for logical verify.

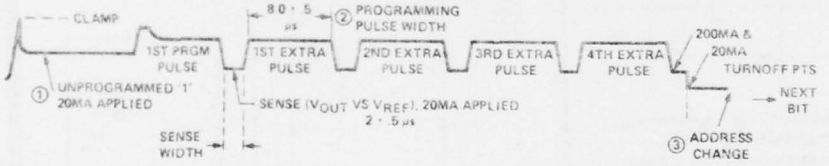
POST PROGRAMMING LOGICAL VERIFICATION

In order to assure data sheet performance of a part under worst case operating conditions, certain test conditions and limits are recommended for logical verification testing after programming.

Both High (V_{OH}) and low (V_{OL}) level should be tested at high (V_{CCH}) and (V_{CCL}) low supply voltages as specified below. During logical verification the enabled state of the part must be established by forcing the specified enabling logical levels on the Chip Enable pins.

CHARACTERISTIC	LIMITS MIN	LIMITS NOM	LIMITS MAX.	UNITS	CONDITIONS
V_{CC} low (4V) Function Test	4.0	4.1	4.2	V	V_{CC} required to perform the "low V_{CC} test"
V out low (Comparator reference) for logical "0"	750	800	850	V	An output is interpreted as a logical "0" when (I_{OL}) 20 ma forcing current produces an output voltage less than the V out low comparator reference
I_{OL} (Force Current)	19.0	20.0	21.0	ma	Constant current source amplitude is adjusted for a nominal value of 20 ma. A resistor load of 40Ω, 1% is used and the source is adjusted for 800mv across the load resistor
V out high (Comparator reference) for logical "1"	4.4	4.5	4.6	V	An output is interpreted as a logical "1" when 100 μa forcing current produces an output voltage greater than the V out high comparator reference
I_{OLK} (force current)	90	100	110	μa	Constant current to be supplied over a 4.4 to 7.1v range adjusted to the nominal value (100 μa)
V_{CC} high (6.5 V) function test	6.4	6.5	6.6	V	V_{CC} required to perform the "V_{CC} high test"
V out low (comparator reference) for logical "0"	750	800	850	V	Refer to V_{CC} low test
I_{OL} (force current)	19.0	20.0	21.0	ma	Refer to V_{CC} low test
V out high (comparator reference) for logical "1"	6.9	7.0	7.1	V	Refer to V_{CC} low test
I_{OLK} (force current)	90	100	110	μa	Refer to V_{CC} low test

TYPICAL VOLTAGE WAVEFORM DURING PROGRAMMING



1. OUTPUT BEING READ FOR PROG/UNPROG BIT, 20MA TURNED ON.
2. NOMINAL PROGRAMMING PULSE WIDTH
3. 20MA SHUTOFF MUST PRECEDE AN ADDRESS CHANGE.

Nichrome Fuse Technology, Vendor A
(Reprinted from vendor borchure)

PROGRAMMING

The Generic PROM's are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROM's can be programmed automatically or by the manual procedure shown below.

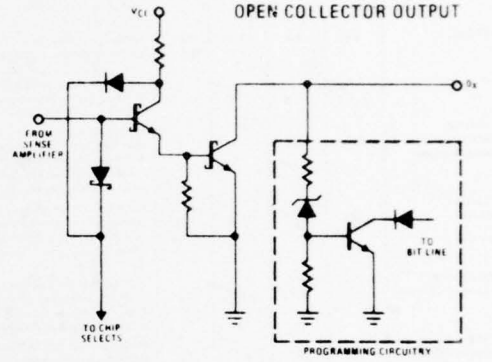
PROGRAMMING SPECIFICATIONS

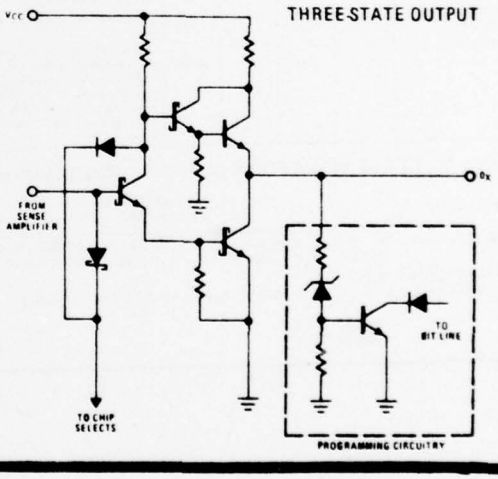
TABLE 1

PARAMETER	SYMBOL	MIN	RECOMMEND VALUE	MAX	UNITS
Address Input Voltage (1)	V_{IH}	2.4	5.0	5.0	V
	V_{IL}	0.0	0.4	0.8	V
Programming/Verify Voltage to V_{CC} (2)	V_{PH}	11.5	12.0	12.5	V
	V_{PL}	3.75	4.0	5.25	
Programming Voltage Current Limit	I_{CCP}			600	mA
Programming (V_{CC}) Voltage Rise and Fall Time	t_r	1	1	10	μs
	t_f	1	1	10	μs
Programming Delay	t_d	10	10	100	μs
Programming Pulse Width First Attempts	t_{p1}	100	100	200	μs
Programming Pulse Width Subsequent	t_{p2}	10	10	20	ms
Programming Duty Cycle	D.C.	-	10	50	%
Output Voltage Enable	V_{OPE}	9.5	10.0	10.5	V
Disable (3)	V_{OPD}	0	4.5	5.5	V
Output Voltage Enable Current Limit	I_{OPE}			10	mA
Case Temp	T_C		25	75	°C

1. Address and chip select should not be left open for V_{IH}.
2. Verification at V_{CC} = 4.0 ± .25 Volts, T_A = 25°C is recommended to guardband performance over full temperature and voltage range.
3. Disable condition will be met with output open circuit.

SCHEMATIC DIAGRAMS





PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying input highs (V_{IH}) to the $\overline{CS}$ input(s). CS inputs (HM-7640/41 only) must remain at V_{IH} for program and verify. The chip select is TTL compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open circuit to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude equal to V_{OPE} and duration of t_{p1} to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to $4.0 \pm .25$ Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ input(s).
9. If any bit does not verify as programmed, repeat steps 2 through 8 using an output enable pulse width of t_{p1} for up to 15 additional pulses to enhance programming speed. If the bit is still unprogrammed, follow with at least 16 repetitive pulses of t_{p2} in width, to achieve high programming yield. In the event that the bit is still unprogrammed, the part is considered a programming reject and should be returned to the factory. The address and incorrect and desired contents of a location in which a programming failure has occured in any returned device must be included with that return.
10. Repeat steps 1 through 9 for all other bits to be programmed in the PROM.

RECOMMENDED PROGRAMMING CIRCUIT

The circuit and timing diagram shown in Figures 1 and 2 will establish the proper programming condition for the output enable pulse. This allows the use of standard TTL parts for all logic inputs to the PROM. Note the gate which senses the output must be input protected to withstand input up to 12.5 Volts during programming.

FIGURE 1

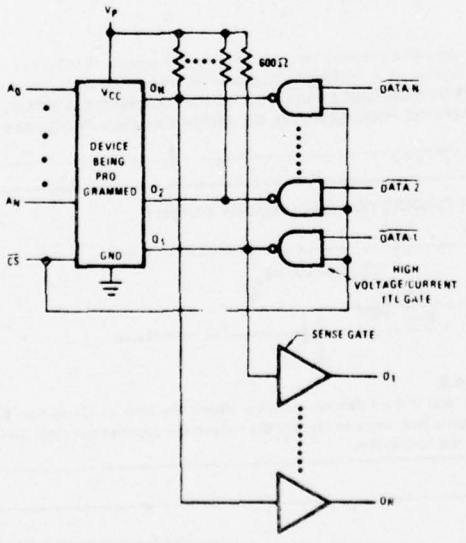
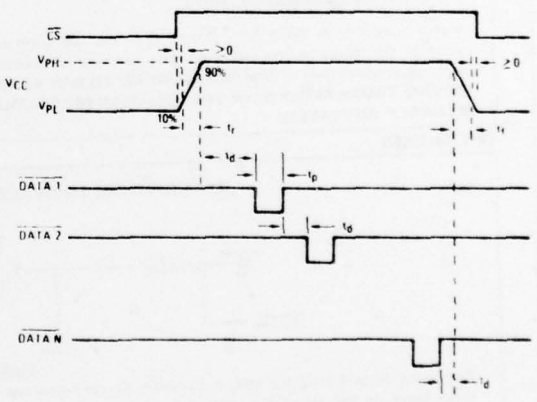


FIGURE 2



Nichrome Fuse Technology, Vendor B
(Reprinted from vendor brochure)

For 1K devices

PROGRAMMING INSTRUCTIONS

1) DEVICE DESCRIPTION

The device is manufactured with all outputs high in all storage locations. To make an output low at a particular word, a nichrome fusible link must be changed from a low resistance to a high resistance. This procedure is called programming. There are 1024 fusible links on the chip. Programming equipment can be obtained from Monolithic Memories Inc.

2) PROGRAMMING DESCRIPTION

To select a particular fusible link for programming, the word address is presented with TTL levels on A_0 through A_7, a V_{CC} of 5.50 V is applied or left applied, and the program pin (Enable $\overline{E}_1$) and the output to be programmed are taken to an elevated voltage to supply the required current to program the fuse. The outputs must be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time.

3) ENABLE $\overline{E}_2$

Enable $\overline{E}_2$ (pin 14) is a logic enable and is not used during programming. It may be high, low or open during programming. When checking that an output is programmed, which is called verification, enables $\overline{E}_1$ and $\overline{E}_2$ must be low to activate the device. Since $\overline{E}_2$ must be low during verification and the state is irrelevant during programming, the simplest procedure is to ground $\overline{E}_2$ during programming and verification.

4) TIMING

The programming procedure involves the use of the program pin (an enable) and the output pin. In order to guarantee that the output transistor is off before increasing the voltage on the output pin, the program pin's voltage pulse must come before the output pin's programming pulse and leave after the output pin's programming pulse. 100 ns delay is adequate. The programming pulse applied to the output pin and program pin must have a 50 to 70 microseconds rise time. See Figure 4.

5) VERIFICATION

After programming a device, it can be checked for a low output by taking both enables low. Since we must guarantee operation at minimum and maximum V_{CC}, load current and temperature, the device must be required to sink 12 mA at 4.20 V V_{CC} and 0.2 mA at 6.0 V V_{CC} at room temperature.

6) BOARD PROGRAMMING

Units may be programmed at the board level by bringing the program pin of each package to the card connector. To program a particular package "A", the program pin of package A and one output of package A, which may or may not be "OR" tied to other packages, are taken to the required programming voltage. An alternate procedure is to tie the enable and outputs together as required by the system function and only apply V_{CC} to the device to be programmed. The number of units soldered on a board should be consistent with expected programming yields to avoid rework.

7) UNPROGRAMMABLE UNITS

Visual inspection at 200X prior to encapsulation, test fuses and decoding circuitry tests are used to guarantee a high programming yield of the device in the field. However, because of random defects, it is impossible to guarantee that a link will open without actually programming it. **UNITS RETURNED TO MMI AS UNPROGRAMMABLE MUST BE ACCOMPANIED BY A COMPLETE DEVICE TRUTH TABLE WITH THE LOCATION WHICH COULDN'T BE PROGRAMMED, OR WHICH FALSELY PROGRAMMED, CLEARLY INDICATED.**

OPERATION

PROGRAMMING EQUIVALENT CIRCUIT FOR ONE MEMORY OUTPUT

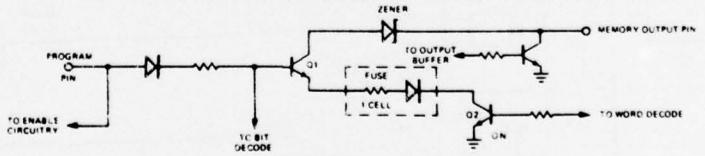


FIGURE 3

The word decode circuitry selects transistor Q_2 to be turned on, and the bit decode circuitry allows the base of Q_1 to rise. 1023 other fuses are half selected or not selected. The program pin supplies base drive to Q_1 and the output pin supplies collector current to Q_1 so that Q_1's emitter can deliver the required current to open the fusible link.

PROGRAMMING INFORMATION

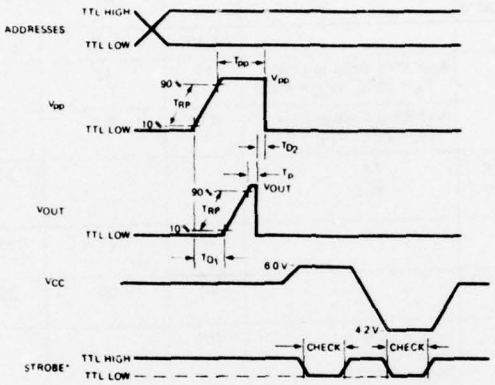
PROGRAMMING SPEED

Typically fuses will blow on the rise time of the pulse.

In automated programmers which must copy devices in a short time because of production requirements, the following pulse and voltage sequences have been found to maximize reliability, programming yield, and thruput. The device should be verified after each programming attempt and is advanced to the next bit if the device has programmed.

PULSE NUMBER	DURATION	PROGRAM PIN VOLTAGE	OUTPUT VOLTAGE
1 to 3	95 μs	27 V	20 V
4 to 6	95 μs	30 V	23 V
7 to 9	95 μs	33 V	26 V

PROGRAMMING TIMING



T_{RP} 60 ± 10 μs
T_{PP} 95 ± 15 μs
T_P 7 ± 1 μs
T_{D_1} 80 ± 10 μs
T_{D_2} 100 ns min.

*NOTE: Output Load = 0.2 mA during 6.0 V check check
Output Load = 12 mA during 4.2 V check

FIGURE 4.

PROGRAMMING INFORMATION

PROGRAMMING PARAMETERS – Do Not Test These Limits or You May Program the Device

SYMBOL	PARAMETERS	TEST CONDITION See Figure 4	LIMITS			UNITS
			MIN.	TYPICAL OR OPTIMUM	MAX.	
I_{pp}	Current into Program Pin During Programming, Before and After Fuse Has Blown	V_{CC} = 5.50 V V_{out} = 5.0 V to 25 V V_{pp} = 4.50 V		0		mA
		V_{pp} = 29 V		77		mA
I_{out}	Current into Output During Programming Before the Fuse Has Programmed	V_{pp} = 29 V, V_{CC} = 5.50 V V_{out} = 9.0 V		0.1		mA
		V_{out} = 20 V		16		mA
I_{out}	Current into Output During Programming After the Fuse Has Programmed	V_{pp} = 29 V, V_{out} = 20 V V_{CC} = 5.50 V		0.1		mA
T_{RP}	Rise Time of Program Pulse Applied to the Data Out or Program Pin From 5 V to 20 V		50	60	70	µs
V_{CCP}	V_{CC} Required During Programming		5.40	5.50	5.60	V
I_{OLV_1}	Output Current Required During Verification	Both Chip Enables Low T_A = 25°C, V_{CC} = 4.2 V	11	12	13	mA
I_{OLV_2}	Output Current Required During Verification	Both Chip Enables Low T_A = 25°C, V_{CC} = 6.0 V	0.19	0.2	0.21	mA
MDC	Maximum Duty Cycle During Automatic Programming of Program Pin and Output Pin	$\frac{T_P}{T_C}$			25	%
V_{pp}	Required Programming Voltage on Program Pin		27	27	33	V
V_{out}	Required Programming Voltage on the Output Pin		20	20	26	V
I_L	Required Current Limit of the Power Supply Feeding the Program Pin and the Output During Programming	V_{pp} = 33 V V_{out} = 26 V V_{CC} = 5.50 V	150			mA
T_{pp}	Required Coincidence Among the Program Pin, Output, Address and V_{CC} for Programming		80	95	110	µs
T_{D_1}	Required Time Delay Between Disabling the Memory Output and Application of the Output Programming Pulse	Measure at 10% Levels	70	80	90	µs
T_{D_2}	Required Time Delay Between Removal of Programming Pulse and Enabling the Memory Output	Measure at 10% Levels	100			ns

SUGGESTED IMPLEMENTATION OF THE VERIFICATION CIRCUITRY

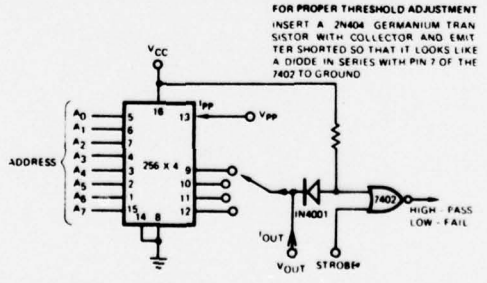


FIGURE 5.
THE 1N4001 DIODE PROTECTS THE INPUT OF THE 7402 FROM THE HIGH PROGRAMMING VOLTAGES

PROGRAMMING INSTRUCTIONS

1) DEVICE DESCRIPTION

The device is manufactured with all outputs high in all storage locations. To make an output low at a particular word, a nichrome fusible link must be changed from a low resistance to a high resistance. This procedure is called programming. There are 2048 fusible links on the chip. Programming equipment can be obtained from Monolithic Memories Inc.

2) PROGRAMMING DESCRIPTION

To select a particular fusible link for programming, the word address is presented with TTL levels on A_0 through A_8, a V_{CC} of 5.50 V is applied or left applied, and the program pin (Enable $\overline{E}_1$) and the output to be programmed are taken to an elevated voltage to supply the required current to program the fuse. The outputs must be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time.

3) TIMING

The programming procedure involves the use of the program pin (an enable) and the output pin. In order to guarantee that the output transistor is off before increasing the voltage on the output pin, the program pin's voltage pulse must come before the output pin's programming pulse and leave after the output pin's programming pulse. 100 ns delay is adequate. The programming pulse applied to the output pin and program pin must have a 50 to 70 microseconds rise time. See Figure 4.

4) VERIFICATION

After programming a device, it can be checked for a low output by taking the enable low. Since we must guarantee operation at minimum and maximum V_{CC}, load current, and temperature, the device must be required to sink 10 mA at 4.20 V V_{CC} and 0.2 mA at 6.0 V V_{CC} at room temperature.

5) BOARD PROGRAMMING

Units may be programmed at the board level by bringing the program pin of each package to the card connector. To program a particular package "A", the program pin of package A and one output of package A, which may or may not be "OR" tied to other packages, are taken to the required programming voltage. An alternate procedure is to tie the enable and outputs together as required by the system function and only apply V_{CC} to the device to be programmed. The number of units soldered on a board should be consistent with expected programming yields to avoid rework.

6) UNPROGRAMMABLE UNITS

Visual inspection at 200X prior to encapsulation, test fuses and decoding circuitry tests are used to guarantee a high programming yield of the device in the field. However, because of random defects, it is impossible to guarantee that a link will open without actually programming it. **UNITS RETURNED TO MMI AS UNPROGRAMMABLE MUST BE ACCOMPANIED BY A COMPLETE DEVICE TRUTH TABLE WITH THE LOCATION WHICH COULDN'T BE PROGRAMMED, OR WHICH FALSELY PROGRAMMED, CLEARLY INDICATED.**

OPERATION

PROGRAMMING EQUIVALENT CIRCUIT FOR ONE MEMORY OUTPUT

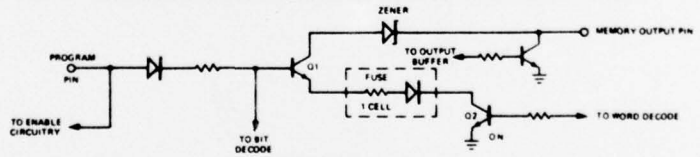


FIGURE 3

The word decode circuitry selects transistor Q_2 to be turned on, and the bit decode circuitry allows the base of Q_1 to rise. 2047 other fuses are half selected or not selected. The program pin supplies base drive to Q_1 and the output pin supplies collector current to Q_1 so that Q_1's emitter can deliver the required current to open the fusible link.

PROGRAMMING INFORMATION

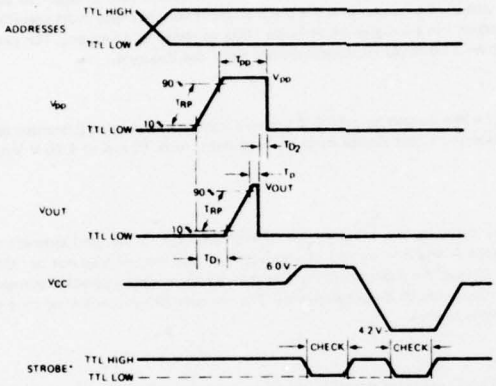
PROGRAMMING SPEED

Typically fuses will blow on the rise time of the pulse.

In automated programmers which must copy devices in a short time because of production requirements, the following pulse and voltage sequences have been found to maximize reliability, programming yield, and thruput. The device should be verified after each programming attempt and is advanced to the next bit if the device has programmed.

PULSE NUMBER	PROGRAM PIN VOLTAGE	OUTPUT VOLTAGE
1 to 3	27 V	20 V
4 to 6	30 V	23 V
7 to 9	33 V	26 V

PROGRAMMING TIMING



T_{RP} 60 ± 10 μs
T_{PP} 95 ± 15 μs
T_P 7 ± 1 μs
T_{D_1} 80 ± 10 μs
T_{D_2} 100 ns min.

*NOTE: Output Load = 0.2 mA during 6.0 V check check
Output Load = 12 mA during 4.2 V check

FIGURE 4.

PROGRAMMING INFORMATION

PROGRAMMING PARAMETERS Do Not Test These Limits or You May Program the Device

SYMBOL	PARAMETERS	TEST CONDITION See Figure 4	LIMITS			UNITS
			MIN.	TYPICAL OR OPTIMUM	MAX.	
I_{pp}	Current into Program Pin During Programming, Before and After Fuse Has Blown	V_{CC} = 5.50 V V_{out} = 5.0 V to 25 V V_{pp} = 4.50 V		0		mA
		V_{pp} = 27 V		150		mA
I_{out}	Current into Output During Programming Before the Fuse Has Programmed	V_{pp} = 27 V, V_{CC} = 5.50 V V_{out} = 9.0 V		0.1		mA
		V_{out} = 20 V		16		mA
I_{out}	Current into Output During Programming After the Fuse Has Programmed	V_{pp} = 27 V, V_{out} = 20 V V_{CC} = 5.50 V		0.1		mA
T_{RP}	Rise Time of Program Pulse Applied to the Data Out or Program Pin From 5 V to 20 V		50	60	70	µs
V_{CCP}	V_{CC} Required During Programming		5.40	5.50	5.60	V
I_{OLV_1}	Output Current Required During Verification	Chip Enable Low T_A = 25°C, V_{CC} = 4.2 V	11	12	13	mA
I_{OLV_2}	Output Current Required During Verification	Chip Enable Low T_A = 25°C, V_{CC} = 6.0 V	0.19	0.2	0.21	mA
MDC	Maximum Duty Cycle During Automatic Programming of Program Pin and Output Pin	$\frac{T_P}{T_C}$			25	%
V_{pp}	Required Programming Voltage on Program Pin		27	27	33	V
V_{out}	Required Programming Voltage on the Output Pin		20	20	26	V
I_L	Required Current Limit of the Power Supply Feeding the Program Pin and the Output During Programming	V_{pp} = 33 V V_{out} = 26 V V_{CC} = 5.50 V	240			mA
T_{pp}	Required Coincidence Among the Program Pin, Output, Address and V_{CC} for Programming		80	95	110	µs
T_{D_1}	Required Time Delay Between Disabling the Memory Output and Application of the Output Programming Pulse	Measure at 10% Levels	70	80	90	µs
T_{D_2}	Required Time Delay Between Removal of Programming Pulse and Enabling the Memory Output	Measure at 10% Levels	100			ns

SUGGESTED IMPLEMENTATION OF THE VERIFICATION CIRCUITRY

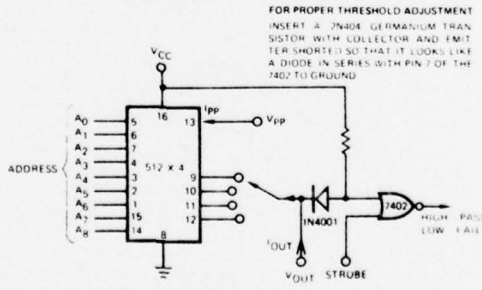


FIGURE 5.
THE 1N4001 DIODE PROTECTS THE INPUT OF THE 7402 FROM THE HIGH PROGRAMMING VOLTAGES

PROGRAMMING INSTRUCTIONS

1) DEVICE DESCRIPTION

The device is manufactured with all outputs high in all storage locations. To make an output low at a particular word, a nichrome fusible link must be changed from a low resistance to a high resistance. This procedure is called programming. Programming equipment can be obtained from Monolithic Memories Inc.

2) PROGRAMMING DESCRIPTION

To select a particular fusible link for programming, the word address is presented with TTL levels on A_0 through A_8, a V_{CC} of 5.50 V is applied or left applied, and the program pin (Enable $\overline{E_2}$) and the output to be programmed are taken to an elevated voltage to supply the required current to program the fuse. The outputs must be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time.

3) ENABLES $\overline{E_1}$, E_3, AND E_4

Enables $\overline{E_1}$, E_3, and E_4 are logic enables and are not used during programming. They may be high, low or open during programming. When checking that an output is programmed (which is called verification) enables $\overline{E_1}$ and $\overline{E_2}$ must be low and E_3 and E_4 must be high to activate the device. Since $\overline{E_1}$ must be low and E_3 and E_4 must be high during verification and their states are irrelevant during programming, the simplest procedure is to ground $\overline{E_1}$ and tie E_3 and E_4 to 5.0 V during programming verification.

4) TIMING

The programming procedure involves the use of the program pin (an enable) and the output pin. In order to guarantee that the output transistor is off before increasing the voltage on the output pin, the program pin's voltage pulse must come before the output pin's programming pulse and leave after the output pin's programming pulse. 100 ns delay is adequate. The programming pulse applied to the output pin and program pin must have a 50 to 70 microseconds rise time. See Figure 4.

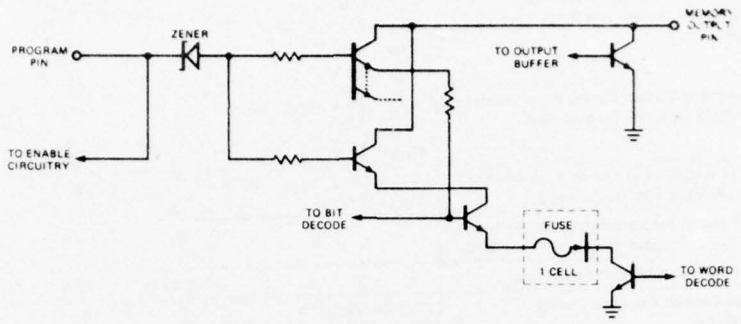
5) VERIFICATION

After programming a device, it can be checked for a low output by taking both enables low. Since we must guarantee operation at minimum and maximum V_{CC}, load current and temperature, the device must be required to sink 12 mA at 4.20 V V_{CC} and 0.2 mA at 6.0 V V_{CC} at room temperature.

6) UNPROGRAMMABLE UNITS

Visual inspection at 200X prior to encapsulation, test fuses and decoding circuitry tests are used to guarantee a high programming yield of the device in the field. However, because of random defects, it is impossible to guarantee that a link will open without actually programming it. **UNITS RETURNED TO MMI AS UNPROGRAMMABLE MUST BE ACCOMPANIED BY A COMPLETE DEVICE TRUTH TABLE WITH THE LOCATION WHICH COULD NOT BE PROGRAMMED, OR WHICH FALSELY PROGRAMMED, CLEARLY INDICATED.**

PROGRAMMING EQUIVALENT CIRCUIT FOR ONE MEMORY OUTPUT



OPERATION

The word decode circuitry selects transistor Q_2 to be turned on, and the bit decode circuitry allows the base of Q_1 to rise. 4095 other fuses are half selected or not selected. The program pin supplies base drive to Q_1 and the output pin supplies collector current to Q_1 so that Q_1's emitter can deliver the required current to open the fusible link.

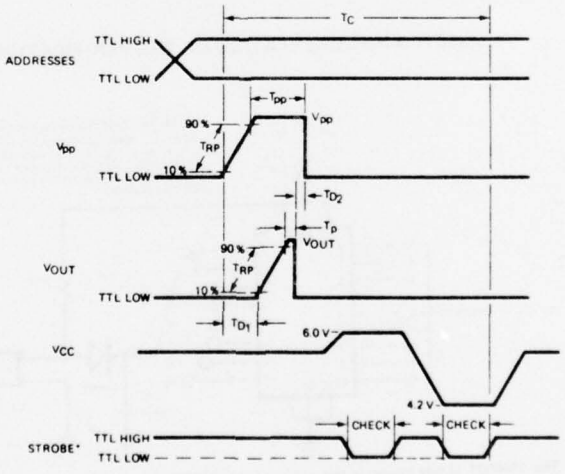
PROGRAMMING SPEED

Typically fuses will blow on the rise time of the pulse.

In automated programmers which must copy devices in a short time because of production requirements, the following pulse and voltage sequences have been found to maximize reliability, programming yield, and thruput. The device should be verified after each programming attempt and is advanced to the next bit if the device has programmed.

PULSE NUMBER	PROGRAM PIN VOLTAGE	OUTPUT VOLTAGE
1 to 3	27 V	20 V
4 to 6	30 V	23 V
7 to 9	33 V	26 V

PROGRAMMING TIMING



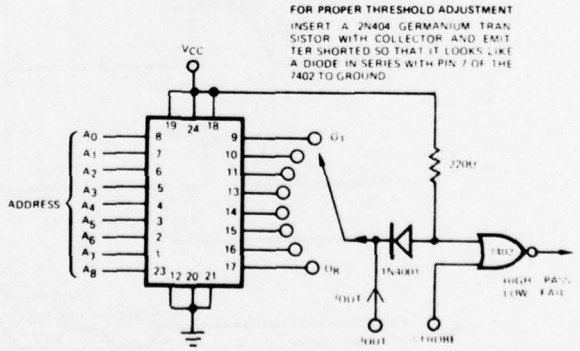
T_{RP} 60 ± 10 µs
T_{PP} 95 ± 15 µs
T_P 7 ± 1 µs
T_{D1} 80 ± 10 µs
T_{D2} 100 ns min.

*NOTE: Output Load = 0.2 mA during 6.0 V check
Output Load = 12 mA during 4.2 V check

PROGRAMMING PARAMETERS Do not test these limits or you may program the device

	PARAMETERS	TEST CONDITION See Figure 4	MIN	TYPICAL OR OPTIMUM	MAX	UNITS
I_{pp}	Current into Program Pin During Programming, Before and After Fuse Has Blown	V_{CC} = 5.50 V V_{out} = 5.0 V to 25 V V_{pp} = 4.50 V		0		mA
		V_{pp} = 27 V		25		mA
I_{out}	Current into Output During Programming Before the Fuse Has Programmed	V_{pp} = 29 V, V_{CC} = 5.50 V V_{out} = 9.0 V		7		mA
		V_{out} = 20 V		50		mA
I_{out}	Current into Output During Programming After the Fuse Has Programmed	V_{pp} = 27 V, V_{out} = 20 V V_{CC} = 5.50 V		35		mA
T_{RP}	Rise Time of Program Pulse Applied to the Data Out or Program Pin from 10% to 90%		50	60	70	µs
V_{CCP}	V_{CC} Required During Programming		5.40	5.50	5.60	V
I_{OLV1}	Output Current Required During Verification	Chip Enabled T_A = 25°C, V_{CC} = 4.2 V	11	12	13	mA
I_{OLV2}	Output Current Required During Verification	Chip Enabled T_A = 25°C, V_{CC} = 6.0 V	0.19	0.2	0.21	mA
MDC	Maximum Duty Cycle During Automatic Programming of Program Pin and Output Pin	$\frac{T_{PP}}{T_C}$			25	%
V_{pp}	Required Programming Voltage on Program Pin		27	27	33	V
V_{out}	Required Programming Voltage on the Output Pin		20	20	26	V
I_L	Required Current Limit of the Power Supply Feeding the Program Pin and the Output During Programming	V_{pp} = 33 V V_{out} = 26 V V_{CC} = 5.50 V	150			mA
T_{pp}	Required Coincidence Among the Program Pin, Output, Address and V_{CC} for Programming		80	95	110	µs
T_{D1}	Required Time Delay Between Disabling the Memory Output and Application of the Output Programming Pulse	Measure at 10% Levels	70	80	90	µs
T_{D2}	Required Time Delay Between Removal of Programming Pulse and Enabling the Memory Output	Measure at 10% Levels	100			ns

SUGGESTED IMPLEMENTATION OF THE VERIFICATION CIRCUITRY



The 1N4001 Diode protects the input of the 7402 from the High Programming Voltages

FIGURE 5

REFERENCES

1. R. C. Smith, S. J. Rosenberg, C. R. Barrett, "Reliability Studies of Polysilicon Fusible Link PROM's," Proc. IEEE 1976 Reliability Physics Symposium (IEEE, NY, 1976), p. 193.

2. "Reliability Evaluation of Programmable Read-Only Memories," Final Technical Report, RADC-TR-75-278, Hughes Aircraft Company for Rome Air Development Center, February 1976.

3. W. Jost, Diffusion in Solids, Liquids, Gases, third printing (Academic Press, NY, 1960), p. 470.

4. G. Parker, J. Cornet, W. Pinter, "Reliability Consi rations in the Design and Fabrication of Polysilicon Fusable Link PROMs," Proc. IEEE 1974 Reliability Physics Symposium (IEEE, NY, 1974), pp. 88-89.

5. B. Pascoe, "Polysilicon Fuse Bipolar PROMs", Intel Reliability Report RR-8 (Intel Corp., October 1975).

6. G. Kenney, W. K. Jones, R. Ogilvie, "Fusing Mechanism of Nichrome-Linked Programmable Read-Only Memory Devices," Proc. IEEE 1976 Reliability Physics Symposium (IEEE, NY, 1976), p. 164.

7. G. B. Kenney, "The Fusing Mechanism of NiCr Resistors in Programmable Read-Only Memory Devices," BS-MS thesis submitted to Dept. of Materials Service and Engineering, MIT, June 1975.

8. W. R. Brockhoff, "Electrically Shorted Semiconductor Junctions Utilized as Programmable Read Only Memory Elements," Proc. IEEE 1976 Reliability Physics Symposium (IEEE, New York, 1976), p. 202.

9. T. M. Donnelly et al., "Reliability Evaluation of Programmable Read-Only Memories (PROMs)," report RADC-TR-75-278 (February 1976).

10. J. McCarthy, "Failure of Aluminum Contacts to Silicon in Shallow Diffused Transistors," Microelectronics and Reliability 9, 187 (1970). See also C. J. Kircher, "Contact Metallurgy for Shallow Junction Si Devices," J. Appl. Phys. 47, 5394 (1976).

11. T. E. Price and L. A. Berthoud, "Aluminum Spearing in Silicon Integrated Circuits," Solid-State Electronics 16, 1303 (1973).

12. E. Philofsky and E. L. Hall, "A Review of the Limitations of Aluminum Thin Films on Semiconductor Devices," IEEE Trans. On Parts, Hybrids, and Packaging PHP-11, 281 (1975).

13. A. Christou, "Electro-thermomigration in Al/Si, Au/Si interdigitized test structures," J. Appl. Phys. 44, 2975 (1973).

14. W. K. Jones, "Plasma Etching as Applied to Failure Analysis," Proc. IEEE 1974 Reliability Physics Symposium (IEEE, NY, 1974), p. 43.

15. J. Davidson, J. Gibson, S. Harris, T. Rossiter, "Fusing Mechanism of Nichrome Thin Films," Proc. IEEE 1976 Reliability Physics Symposium (IEEE, NY, 1976), p. 173.

16. H. C. Rickers, "Microcircuit Device Reliability: Memory/LSI Data", Reliability Analysis Center report MDR-3 (Rome Air Development Center, Winter 1975-1976).

17. R. C. Smith, S. J. Rosenberg, and C. R. Barrett, "Reliability Studies of Polysilicon Fusible Link PROM's", Proc. IEEE 1976 Reliability Physics Symposium (IEEE, N. Y., 1976); Bill Pascoe, "Polysilicon Fuse Bipolar PROMs," Intel report RR-9 (Intel Corp, Santa Clara, CA, 1975).

18. D. G. Platteter (Naval Weapons Support Center, Crane, Indiana), private communication (July 1975).

19. P. G. Shewmon, Diffusion in Solids (McGraw-Hill, N. Y., 1963).

20. P. Franklin, "A Reliability Assessment of Bipolar PROMs," Proc. IEEE 1976 Reliability Physics Symposium (IEEE, N. Y., 1976.)

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